# 國立中興大學電機資訊學院

## 院長候選人登記應繳交表格及相關證件清單

### (請依序逐項檢齊----所送影本均請候選人簽章以資確認)

姓名： 張振豪　　　　　　　現職單位及職稱：電機系特聘教授


■國立中興大學電機資訊學院院長候選人資料表。(正本)

■教授證書影本。

■資料表所載明資料之相關學經歷證明文件。

□候選人推薦表（自行登記參選者免附推薦表）。

■中華民國身分證或護照影本。

■最近五年於列名 JCR 之國際期刊發表論文〔含發明專利、新品種育成、技術移轉等成果〕三篇(件)(第一作者或通訊作者)以上者。

■最近五年曾主持三年以上國家科學及技術委員會研究型計畫者。

□最近五年曾獲校級教學或服務特優獎勵者。

■其他有助於審查資格之資料。

■未曾因違反學術倫理而受校教師評審委員會處分。


候選人親筆簽名：＿＿張振豪＿＿

113 年　4　月　15　日

# 國立中興大學電機資訊學院院長候選人資料表

## 壹. 個人基本資料

| 姓　　名 | 別　　號 | 性別 | 出生年月日 | 國　　籍 | 電　　話 | 傳　　真 |
|---|---|---|---|---|---|---|
| 張振豪 | | 男 | 民國 54 年 5 月 ■ 日 | 中華民國 | 公：04-22851549#263<br>宅：■ | 公：04-22851410<br>宅： |

通訊處：台中市興大路 145 號 國立中興大學電機系

E - mail：chchang@nchu.edu.tw

個人網頁：
http://www.ee.nchu.edu.tw/index.asp?url=32&cno=5&tno=25

### 現職

| 服 務 機 關 名 稱 | 專 兼 任 | 職 稱 （ 職 級 ） | 到職年月日 |
|---|---|---|---|
| 國立中興大學電機系 | 專任 | 特聘教授 | 85 年 8 月 1 日 |

### 大學以上學歷

| 學 校 名 稱 | 院 系 所 | 學 位 名 稱 | 領受學位年月 |
|---|---|---|---|
| 美國南加州大學 | 電機系 | 博士 | 1995 年 5 月 |
| 國立台灣大學 | 電機系 | 碩士 | 1989 年 6 月 |
| 國立台灣大學 | 電機系 | 學士 | 1987 年 6 月 |
| | | | |
| | | | |

### 經歷

| 服 務 機 關 名 稱 | 專 兼 任 | 職 稱 （ 職 級 ） | 任職起迄年月 |
|---|---|---|---|
| 國科會工程處微電子學門 | 兼任 | 召集人 | 2024/1~目前 |
| 國科會國家核心關鍵技術辦公室 | 兼任 | 核心諮詢委員 | 2023/5~目前 |
| 國科會臺灣 AI 卓越中心(Taiwan AI Center of Excellence) | 兼任 | 策略委員 | 2022/10~目前 |
| 國科會科技政策諮詢專家室智慧資通群組 | 兼任 | 領域專家 | 2022/8~目前 |
| 國立中興大學電機系 | 專任 | 教授 | 2003/8~目前 |
| 國家科學及技術委員會半導體射月計畫 | 兼任 | 專案召集人 | 2018/1～2022/6 |
| 國立暨南國際大學科技學院 | 專任（借調） | 院長 | 2014/8～2017/7 |
| 國研院國家晶片系統設計中心（CIC） | 兼任 | 副主任 | 2011/3～2014/1 |

| 教育部「智慧電子整合性人才培育計畫」-先導教學平台(ATP)推 | 兼 任 | 召集人 | 2011/3 ~ 2016/4 |
|---|---|---|---|
| IEEE Circuits and Systems Society, Taipei Chapter | 兼 任 | 分會 主席 | 2011/1 ~ 2012/12 |
| 國立中興大學電機系 | 兼 任 | 系主任 | 2006/8 ~ 2008/7 |
| 國立中興大學工學院工科中心 | 兼 任 | 主任 | 2005/8 ~ 2006/7 |
| 國立中興大學電機系 | 專 任 | 副教授 | 1996/8 ~ 2003/7 |

註：1.請附最高學歷及教授或相當於教授資格之證件影本。

2.個人網頁資料之正確性由候選人負責確認。

候選人親筆簽名：　張振豪

| 內　　　　　　　　　　　　　　　　　容 | 時　　間 |
|---|---|
| 1. 中國電機工程學會，109 年「**傑出電機工程教授獎**」 | 2020/10 |
| 2. 國立中興大學**終身特聘教授** | 2020/8~ |
| 3. 「智慧電子國家型科技計畫(NPIE)」**卓越計畫獎**(計畫名稱：智慧行車安全監控嵌入式系統設計) | 2015 |
| 4. 國立中興大學 103 學年度工學院「**產學合作優良獎**」 | 2015/1 |
| 5. 教育部大專院校實施**特殊優秀人才彈性薪資**方案 | 2014/12~2017/7 |
| 6. IEEE Circuits and Systems Society (CASS), **Distinguished Lecturer** | 2013/1~2014/12 |
| 7. 國立中興大學**特聘教授** | 2012/2~2016/1 2020/8~ |
| 8. The Institution of Engineering and Technology, **Fellow** | 2011/9 |
| 9. 100 年度**產學績優教師 I**(全校產學績分排名前 2%之教師) | 2011 |
| 10. 國立中興大學九十八學年度電機系**優良教師**選拔第一名 | 2010/5 |
| 11. 國立中興大學九十八學年度「**工學院產學合作優良獎**」 | 2009 |
| 12. 國立中興大學工學院九十七學年度**教師評鑑特優獎** | 2008 |
| 13. 國立中興大學 94 年度**建教合作研究計畫教師績優獎** | 2005 |
| 14. 國立中興大學**教學特優教師獎** | 2004 |
| 15. 國際 **Tau Beta Pi** 榮譽學會會員 | 1995 |
| 16. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, **Senior Editorial Board** (2020~2021) **& Lead Guest Editor** (2019) | 2020/1~2021/12 & 2019/12 |
| 17. IEEE Journal of Solid-State Circuits 之 **Lead Guest Editor (2021)及 Guest Editor(2019)** | 2021/10 & 2019/10 |
| 18. IEEE Trans. on VLSI Systems, **Associate Editor** | 2010/1~2014/12 |
| 19. IEEE International Symposium on Circuits and Systems, **Plenary Chair** | 2021/5 |

| | | |
|---|---|---|
| 20. | IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS 2019), **Founding General Chair** | 2019/3 |
| 21. | IEEE Asian Solid-State Circuits Conference (A-SSCC), **Technical Program Committee Chair** (2020)/ **TPC Co-Chair** (2019)/ **Sub-Committee Chair** (2015~2018)/ **Technical Program Committee Member** (2011~2014, 2021~2023) | 2011~2022 |
| 22. | The 22nd VLSI Design/CAD Symposium, **General Chair** | 2011/8 |
| 23. | IEEE CAS Society, Nanoelectronics & Gigascale Systems, Technical Committee (NG-TC), **Chair** (2015/7~2017/6), **Chair-Elect** (2013/7~2015/6), **Secretary** (2011/7~2013/6), **Technical Committee Member** (2009~) | 2009~ |
| 24. | IEEE Systems Council, **AdCom Member** (Circuits and Systems Society Primary Representative) | 2016/1~2019/12 |
| 25. | 臺灣半導體產學研發聯盟(TIARA)**副理事長** | 2022/6~2024/5 |
| 26. | 台灣人工智慧晶片聯盟(AI-on-Chip Taiwan Alliance, AITA) **AI 系統應用 SIG 主席** | 2019/1~ |
| 27. | 中華民國台灣半導體產業協會(TSIA) **產學委員會委員** | 2018/1~ |
| 28. | 台灣積體電路設計學會 **監事** (2014/8~2018/7)、**常務理事** (2010/8~2014/7)、**理事**(2004/8~2008/7) | 2004/8~2018 |
| 29. | 擔任國家科學及技術委員會**半導體射月計畫專案召集人**，推動全國智慧終端半導體製程與晶片系統研發(**總經費為 27.55 億元**)，補助台、成、清、交等全國 20 群菁英研究團隊之頂尖研究，挑戰 2022 年智慧終端(AI Edge)關鍵技術極限。 | 2018~2022 |
| 30. | 擔任教育部「智慧電子整合性人才培育計畫」-**先導教學平台(ATP)推動中心召集人**，負責全國各大學智慧電子課程推廣教學計畫之審查與考核(總經費約 4 億元)，奠定我國高階跨領域智慧電子前瞻課程。 | 2011/3~2016/4 |

註：本表若不敷使用請自行影印

候選人親筆簽名：張振豪

期刊論文：

[1] C.-Y. Yang, C.-H. Lin, R. C.-H. Chang, and S. Palermo, "A 17.5-to-21-GHz current-folding frequency tripler with >36-dBc harmonic rejection in 90-nm CMOS," *IEEE Solid-State Circuits Letters*, vol. 6, no. 3, pp. 77-80, Mar. 2023. (SCI)

[2] R. C.-H. Chang, C.-Y. Wang, Y.-H. Li, and C.-D. Chiu, "Design of low-complexity convolutional neural network accelerator for finger vein identification system," *Sensors* 2023, vol. 23, no. 4, 2184; https://doi.org/10.3390/s23042184 (registering DOI) - 15 Feb. 2023. (SCI)

[3] R. C.-H. Chang, C.-Y. Wang, W.-T. Chen, and C.-D. Chiu, "Drowsiness detection system based on PERCLOS and facial physiological signal," *Sensors 2022*, vol. 22, no. 14, 5380; https://doi.org/10.3390/s22145380 (registering DOI) - 19 Jul. 2022. (SCI)

[4] R. C.-H. Chang, C.-Y. Wang, H.-H. Li, and C.-D. Chiu, "Drunk driving detection using two-stage deep neural network," *IEEE Access*, vol. 9, pp. 116564 – 116571, Aug. 2021. (SCI)

[5] C.-Y. Wang, C.-H. Tsai, S.-C. Wang, C.-Y. Wen, R. C.-H. Chang, C.-P. Fan, "Design and implementation of lora-based wireless sensor network with embedded system for smart agricultural recycling rapid processing factory," *IEICE Trans. on Information and Systems*, vol. E104-D, no.5, pp.563-574, May 2021. (SCI)

[6] M.-F. Chang, C. Lin, C. H. Shen, S. W. Wang, K. C. Chang, R. C.-H. Chang and W. K. Yeh, "The role of government policy in the building of a global semiconductor industry," *Nature Electronics*, vol. 4, pp. 230-233, Apr. 2021. (SCI)

[7] R. C.-H. Chang, W.-C. Chen, and S.-C. Su, "Compensator-free Li-ion battery charger with current window control," *IEICE Transactions on Electronics*, vol. E104-C, no.3, pp. 128-131, Mar. 2021. (SCI)

[8] R. C.-H. Chang, W.-C. Chen, and J. K.-S. Huang, "A 93.4% efficiency 8mV offset voltage constant on-time buck converter with an offset cancellation technique," *IEEE Trans. on Circuits and Systems – II*, vol. 67, no. 10, pp. 2069 – 2073, Oct. 2020. (SCI)

[9] R. C.-H. Chang, W.-C. Chen, L. Liu, and S.-H. Cheng, "An AC–DC rectifier with active and non-overlapping control for piezoelectric vibration energy harvesting," *IEEE Trans. on Circuits and Systems – II*, vol. 67, no. 6, pp. 969-973, June 2020.

會議論文：

[1] C.-Y. Wang, M.-Z. Zhong, S.-C. Wang, R. C.-H. Chang, and C.-Y. Wen, "LoRa-based hierarchical network architecture for IoT indoor positioning applications," *2023 IEEE International Conference on Consumer Electronics - Taiwan*, July 2023.

[2] R. C.-H. Chang, C.-Y. Wang, and Y.-Y. Kao, "Implementation of a novel intelligent drowsiness detection warning system," *2021 IEEE International Conference on Consumer Electronics - Taiwan*, Sept. 2021.

[3] R. C.-H. Chang, W.-C. Chen, and J. K.-S. Huang, "A 93.4% efficiency 8mV offset voltage constant on-time buck converter with an offset cancellation technique," *IEEE Intl. Symp. on Circuits and Systems*, Daegu, Korea & Virtual Platform, May 2021. (EI)

[4] Y.-C. Hsu and R. C.-H. Chang "Intelligent chips and technologies for AIoT era," *IEEE Asian Solid-State Circuits Conference*, Hiroshima, Japan, (virtual) Nov. 2020.

[5] R. C.-H. Chang, P.-S. Lei, K.-S. Huang and W.-C. Chen, "Batteryless DC-DC boost converter for thermoelectric energy harvesting devices," *The 17th International SoC Design Conference (ISOCC)*, Yeosu, Korea, Oct. 2020. (Best paper award)

[6] Y.-H. Chen, C.-P. Fan, and R. C.-H. Chang, "Prototype of low complexity CNN hardware accelerator with FPGA-based PYNQ Platform for dual-mode biometrics recognition," *The 17th International SoC Conference*, Yeosu, Korea, Oct. 2020.

[7] R. C.-H. Chang, W.-C. Chen, L. Liu, and S.-H. Cheng, "An AC–DC rectifier with active and non-overlapping control for piezoelectric vibration energy harvesting," *IEEE Intl. Symp. on Circuits and Systems*, Sevilla, Spain, (virtual) Oct. 2020. (EI).

[8] C.-W. Chuang, C.-P. Fan and R. C.-H. Chang, "Design of low-complexity yolov3-based deep-learning networks with joint Iris and Sclera messages for biometric recognition application," *IEEE 9th Global Conference on Consumer Electronics*, Kobe, Japan, Oct. 2020.

[9] R. C.-H. Chang, C.-Y. Wang, and C.-H. Shen, "Modified YOLOv3-tiny using dilated convolution for driver distraction detection," *2020 IEEE International Conference on Consumer Electronics - Taiwan*, Oct. 2020.

[10] C.-W. Chuang, C.-P. Fan, and R. C.-H. Chang, "Comparison and study of yolov2-based deep-learning networks without Iris and Sclera segmentation for biometric authentication," *The 31st VLSI Design/CAD Symposium*, Kaohsiung, Taiwan, Aug. 2020.

專利:

[1] 張振豪、陳泓烈，"手掌靜脈特徵辨識系統及其方法，" 中華民國發明專利，第 I781459 號，專利期間:2022 年 10 月 21 日~ 2040 年 10 月 7 日。

[2] 張振豪、李欣翰、馬德芸，"狀態辨識系統與方法，" 中華民國發明專利，第 I758665 號，專利期間:2022 年 3 月 21 日~ 2039 年 12 月 4 日。

[3] 張振豪、王佳裕，"電力變壓器之故障診斷監控系統，" 中華民國發明專利，第 I739634 號，專利期間:2021 年 9 月 11 日~ 2040 年 10 月 15 日。

[4] 張振豪、張智瑋、王佳裕，"指/掌靜脈辨識處理及其神經網路訓練方法，" 中華民國發明專利，第 I731511 號，專利期間:2021 年 6 月 21 日~ 2039 年 12 月 11 日。

[5] 張振豪、陳威志、劉霖，"全整合主動式交流轉直流整流器，" 中華民國發明專利，第 I677179 號，專利期間:2019 年 11 月 11 日~ 2038 年 11 月 28 日。

註：本表若不敷使用請自行影印

候選人親筆簽名：張振豪

　　國立中興大學電機資訊學院，成立於民國107年，是一所結合理論與實務、跨領域學習的優質教育機構。學院匯集了電機、資訊、通訊、光電等多個領域的專業知識，依專業性質可分為智慧感知與資訊應用、行動通訊與智慧物聯網、智慧電子與光電系統、智慧系統與晶片設計及智慧型控制與應用等五領域，發展完整而強健的電機資訊體系。

　　學院積極投入人才養成、學術研究、以及扶植產業的角色，期能對我國電機資訊產業的升級和科技發展有所貢獻。學院不僅提供學士、碩士、博士等多層次的教育，並設有在職專班，以滿足不同學習需求。學院目前核配之師資總員額為56名，包括專任教師54名、兼任教師員額2名，擁有玉山學者、講座教授、特聘教授等優秀師資，提供學生豐富的學習資源與研究機會。

　　學院也與國際知名大學建立合作關係，進行學術交流與研究合作，並提供學生海外學習的機會。本院在楊院長及全體教師努力下，已為本院奠定了相當良好的基礎，以卓越的教學品質、創新的研究成果和積極的產學合作，成為培育未來電資領域專業人才的重要搖籃。以下針對教學、研究及行政服務等三部份來說明本人對未來院務發展的理念：


# 一、教學

1. 延聘國內外優秀師資，以提升本院教學研究品質與成果。

2. 加強招生宣傳，如：豐富中英文網頁資訊、對高中師生open house等。

3. 強化與高中之互動，協助指導學生參加國內外科展。

4. 協助及鼓勵各系所招收國際學生。

5. 推動與與歐美日等大學辦理雙聯學位。

6. 鼓勵學生參與國際交流活動或交換學生計畫，以拓展學生國際視野。

7. 協助學生參與業界暑期實習工作，增進學生理論與實務結合的能力。

8. 積極培育產業所需的電資領域高階人才。

9. 輔導學生參與國內外政府或民間舉辦的各項競賽。

10. 開設或推廣跨領域專業學程，以培育具多元專業能力及跨領域專長的學生。


## 二、研究

1. 晶創台灣計畫是由國科會於2023年啟動的一項重大計畫，該計畫將結合生成式人工智慧(AI)與半導體晶片設計製造的優勢，來驅動台灣未來在食、醫、住、行、育、樂、工業等全產業創新發展，同時也要強化國內培育環境吸納全球研發人才、加速產業創新所需異質整合及先進技術、及利用矽島實力吸引國際新創與投資來台。本院可配合該計畫之發展，並爭取各部會整合型或大型研究計畫。

2. 協助各系所針對最新研究主題進行規劃，組成研究團隊，如: 6G、無人機、生成式AI、智慧機器人、前瞻半導體、高算力晶片、異質整合、量子運算、資安...等。

3. 協助各系所建立優良的學術研究環境，以提昇本院學術水準與研究能量。

4. 鼓勵教師除了發表學術論文外，可多嘗試撰寫學術性專書及專章著作或發表專利。

5. 鼓勵教師參與國際性學術組織，並爭取擔任國際重要期刊編輯及主辦國際會議，以提升本院及各系所國際知名度。

6. 邀請國外學者來訪，以增加國際學術交流及研究合作的機會。

7. 協助教師進行產學交流及校外研究單位之合作。

8. 鼓勵學生參與教授研究計畫或申請國科會大專生研究計畫。


## 三、行政服務

1. 擔任各系所溝通協調的橋樑，以公平、公開、公正之原則處理院務。

2. 合理分工、充份授權，以提升行政效率並落實行政支援教學及研究發展。

3. 協助各系所爭取教學研究資源與空間。

4. 發行「電資學院電子報」報導院內及各系所教學、研究、課外活動等訊息，以增

進跨系所師生、院友間的溝通及了解。

5. 獎勵及表揚教授之傑出表現，並積極推薦本院同仁參與各種獎項之甄選，以提高本院在國內外的知名度。

6. 舉辦院內聯誼活動，以增加院內同仁交流的機會，並促進院內和諧。

候選人親筆簽名：張振豪

# 國立中興大學電機資訊學院院長候選人

## 最近五年符合本校院長遴選、續聘、及解聘辦法第 5 條第 2 項之資格條件一覽表

院長候選人是否曾因違反學術倫理而受校教評會處分。□是 ■否

符合院長候選人資格條件勾選(須符合以下條件之一,並檢附佐證資料)

| 候選人姓名 | 符合條件(請勾選)及相關內容 |
|---|---|
| 張振豪 | ■於各學院認可之國際期刊發表論文〔含發明專利、新品種育成、技術移轉等成果〕三篇(件)(第一作者或通訊作者)以上。文學院、管理學院及法政學院包含國家科學及技術委員會各學門之一級期刊或國際期刊對等之論文集論文二篇以上,或由具審查制度之出版單位且經院教評會審查通過出版專書一本以上。<br><br>■曾主持三年以上國家科學及技術委員會研究型計畫者。文學院、管理學院及法政學院最近五年曾主持二年以上國家科學及技術委員會研究型計畫者。<br><br>□曾獲校級教學或服務特優獎勵者。<br><br>【前述之著作均須符合本校「教師升等評審標準暨聘任升等著作送審準則」之規定。】<br><br>※相關資格條件敘明如下: |

國際期刊論文:

[1] **R. C.-H. Chang**, C.-Y. Wang, Y.-H. Li, and C.-D. Chiu, "Design of low-complexity convolutional neural network accelerator for finger vein identification system," *Sensors* 2023, vol. 23, no. 4, 2184; https://doi.org/10.3390/s23042184 (registering DOI) - 15 Feb. 2023. (SCI)

[2] **R. C.-H. Chang**, C.-Y. Wang, W.-T. Chen, and C.-D. Chiu, "Drowsiness detection system based on PERCLOS and facial physiological signal," *Sensors 2022*, vol. 22, no. 14, 5380; https://doi.org/10.3390/s22145380 (registering DOI) - 19 Jul. 2022. (SCI)

[3] **R. C.-H. Chang**, C.-Y. Wang, H.-H. Li, and C.-D. Chiu, "Drunk driving detection using two-stage deep neural network," *IEEE Access*, vol. 9, pp. 116564 – 116571, Aug. 2021. (SCI)

[4] **R. C.-H. Chang**, W.-C. Chen, and S.-C. Su, "Compensator-free Li-ion battery charger with current window control," *IEICE Transactions on Electronics*, vol. E104-C, no.3, pp. 128-131, Mar. 2021. (SCI)

[5] **R. C.-H. Chang**, W.-C. Chen, and J. K.-S. Huang, "A 93.4% efficiency 8mV offset voltage constant on-time buck converter with an offset cancellation technique," *IEEE Trans. on Circuits and Systems – II*, vol. 67, no. 10, pp. 2069 – 2073, Oct. 2020. (SCI)

[6] **R. C.-H. Chang**, W.-C. Chen, L. Liu, and S.-H. Cheng, "An AC–DC rectifier with active and non-overlapping control for piezoelectric vibration energy harvesting," *IEEE Trans. on Circuits and Systems – II*, vol. 67, no. 6, pp. 969-973, June 2020.

國家科學及技術委員會研究型計畫

| 計畫名稱 | 起訖年月 | 經費總額 |
|---|---|---|
| 應用於生理感測之高解析度雜訊整形逐次逼近類比數位轉換器 | 2023/08/01~2024/07/31 | 648,000 |
| 應用於第六代通訊之小晶片異質整合的每秒兆位元全雙工收發器(2/4) | 2023/05/01~2024/04/30 | 8,500,000 |
| 應用於第六代通訊之小晶片異質整合的每秒兆位元全雙工收發器(1/4) | 2022/05/01~2023/04/30 | 9,770,000 |

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|---|---|---|---|
| | 低功率生理感測電路設計(II) | 2021/08/01~2022/07/31 | 1,352,000 |
| | 無線低功率安全偵測單晶片系統設計-總計畫暨子計畫一：低功率生理感測電路設計 | 2020/08/01~2021/10/31 | 2,562,000 |
| | 人工智慧監控與辨識系統:應用於身份辨識之低功率深度學習可重組加速器晶片-人工智慧監控與辨識系統:應用於身份辨識之低功率深度學習可重組加速器晶片(3/3) | 2019/06/01~2020/05/31 | 4,500,000 |
| | 基於深度學習之手掌靜脈辨識及其硬體加速器之設計 | 2019/08/01~2020/07/31 | 997,000 |
| | 基於深度學習之手掌靜脈辨識及其硬體加速器之設計 | 2018/08/01~2019/07/31 | 997,000 |
| | 人工智慧監控與辨識系統:應用於身份辨識之低功率深度學習可重組加速器晶片-人工智慧監控與辨識系統:應用於身份辨識之低功率深度學習可重組加速器晶片(2/3) | 2018/06/01~2019/05/31 | 4,960,000 |
| | 總計 | | 34,286,000 |

附註：

一、國立中興大學院長遴選、續聘、及解聘辦法第5條第2項規定：「前項候選人應為學養俱佳、教學認真、公正、熱心之教授，且須有下列各款條件之一：一、最近五年於各學院認可之國際期刊發表論文〔含發明專利、新品種育成、技術移轉等成果〕三篇(件)(第一作者或通訊作者)以上。文學院、管理學院及法政學院包含國家科學及技術委員會各學門之一級期刊或國際期刊對等之論文集論文二篇以上，或由具審查制度之出版單位且經院教評會審查通過出版專書一本以上。二、最近五年曾主持三年以上國家科學及技術委員會研究型計畫者。文學院、管理學院及法政學院最近五年曾主持二年以上國家科學及技術委員會研究型計畫者。三、最近五年曾獲校級教學或服務特優獎勵者。」又第3項規定：「前述之著作均須符合本校「教師升等評審標準暨聘任升等著作送審準則」之規定。」

二、請依符合之條件敘明相關內容：

　　1.於各學院認可之國際期刊發表論文：請敘明作者、論文名稱、出版處所、出版年月、頁次。

　　2.專書一本(含)以上(文學院、管理學院及法政學院)：請敘明作者、專書名稱、出版處所、出版年月。

　　3.曾主持國家科學及技術委員會研究型計畫者：請敘明計畫名稱、時間。

　　4.曾獲校級教學或服務特優獎勵者：請敘明獲獎時間。

三、本表若不敷使用請自行增加列數，並請註記頁次。

候選人親筆簽名：　張振豪

# Design of Low-Complexity Convolutional Neural Network Accelerator for Finger Vein Identification System

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**Abstract:** In the biometric field, vein identification is a vital process that is constrained by the invisibility of veins as well as other unique features. Moreover, users generally do not wish to have their personal information uploaded to the cloud, so edge computing has become popular for the sake of protecting user privacy. In this paper, we propose a low-complexity and lightweight convolutional neural network (CNN) and we design intellectual property (IP) for shortening the inference time in finger vein recognition. This neural network system can operate independently in client mode. After fetching the user's finger vein image via a near-infrared (NIR) camera mounted on an embedded system, vein features can be efficiently extracted by vein curving algorithms and user identification can be completed quickly. Better image quality and higher recognition accuracy can be obtained by combining several preprocessing techniques and the modified CNN. Experimental data were collected by the finger vein image capture equipment developed in our laboratory based on the specifications of similar products currently on the market. Extensive experiments demonstrated the practicality and robustness of the proposed finger vein identification system.

**Keywords:** finger vein; CNNs; batch normalization; SDUMLA-HMT; contrast limited adaptive histogram equalization (CLAHE)

## 1. Introduction

Security verification technologies have advanced rapidly in modern society. For example, airport check-in systems have advanced from manual to automatic inspections. With the increasing focus on personal privacy, much attention has been paid to biometric verification, which utilizes human physiological characteristics, such as features of the sclera [1], fingerprints [2], veins [1,3,4], and face [5], for identity verification. All these technologies have three things in common. First, every person has their own biometrics (i.e., "uniqueness"). Second, these features do not change dramatically over time (i.e., "stability"). Lastly, users need not bring all their personal keycards with them, and these biometric features allow accurate identification and are hard to spoof or steal (i.e., "safety and portability"). With these three advantages, biometrics has become the main trend for personal identification in modern society.

Finger vein features used in human recognition methods, whether it is image processing of photographic devices or finger vein feature recognition algorithms, have been implemented in various applications that require security, such as ATMs and security doors [6,7]. The finger vein identification system recognizes the structure of the visible blood vessel pattern in the finger, which can only be irradiated with near-infrared (NIR) light wavelengths. Because finger vein patterns are located under the skin, they are

# Drowsiness Detection System Based on PERCLOS and Facial Physiological Signal [†]

Robert Chen-Hao Chang [1,2,*], Chia-Yu Wang [1], Wei-Ting Chen [1] and Cheng-Di Chiu [3,*]

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[†] This paper is an extended version of our paper published in: Chang, R.C.-H.; Wang, C.-Y.; Kao, Y.-Y. Implementation of a Novel Intelligent Drowsiness Detection Warning System. In the Proceedings of the IEEE International Conference on Consumer Electronics—Taiwan (IEEE 2021 ICCE-TW), Penghu, Taiwan, 15–17 September 2021.

**Abstract:** Accidents caused by fatigue occur frequently, and numerous scholars have devoted tremendous efforts to investigate methods to reduce accidents caused by fatigued driving. Accordingly, the assessment of the spirit status of the driver through the eyes blinking frequency and the measurement of physiological signals have emerged as effective methods. In this study, a drowsiness detection system is proposed to combine the detection of LF/HF ratio from heart rate variability (HRV) of photoplethysmographic imaging (PPGI) and percentage of eyelid closure over the pupil over time (PERCLOS), and to utilize the advantages of both methods to improve the accuracy and robustness of drowsiness detection. The proposed algorithm performs three functions, including LF/HF ratio from HRV status judgment, eye state detection, and drowsiness judgment. In addition, this study utilized a near-infrared webcam to obtain a facial image to achieve non-contact measurement, alleviate the inconvenience of using a contact wearable device, and for use in a dark environment. Furthermore, we selected the appropriate RGB channel under different light sources to obtain LF/HF ratio from HRV of PPGI. The main drowsiness judgment basis of the proposed drowsiness detection system is the use of algorithm to obtain sympathetic/parasympathetic nervous balance index and percentage of eyelid closure. In the experiment, there are 10 awake samples and 30 sleepy samples. The sensitivity is 88.9%, the specificity is 93.5%, the positive predictive value is 80%, and the system accuracy is 92.5%. In addition, an electroencephalography signal was used as a contrast to validate the reliability of the proposed method.

**Keywords:** PERCLOS; drowsiness detection; sympathetic nervous index; parasympathetic nervous index; EEG

## 1. Introduction

In 2014, the National Highway Traffic Safety Administration (NHTSA), United States Department of Transportation [1] recorded 846 fatalities caused by drowsy driving, and this number is almost equal to the past 10 years. According to Finnish statistics, 16% of the fatal accidents involving connected vehicles are caused by fatigued driving [2]. Accordingly, accidents caused by fatigued driving can be reduced by developing a method to issue appropriate warnings to fatigued drivers.

Several studies have been reported regarding electrophysiological signals that can be used for drowsiness detection. For example, the HSV and mIIR algorithm was developed for the realization of the robust heart rate estimation system from webcam based face color image [3]. Qian et al. proposed a model of Bayesian non-negative CP decomposition

# Drunk Driving Detection Using Two-Stage Deep Neural Network

## ROBERT CHEN-HAO CHANG[ID]1, (Senior Member, IEEE), CHIA-YU WANG[ID]1, HSIN-HAN LI[ID]1, AND CHENG-DI CHIU[ID]2

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**ABSTRACT** Drunk driving accidents have been rapidly increasing in recent times. Although the statistics show a decreasing trend in recent years, reports of drunk driving accidents are often seen in the news. To assess vehicle operators for drunk driving, the police still use breath-alcohol testers as the primary method. However, a certified instrument to measure alcohol consumption is expensive, and the mouthpiece used in the instrument is a consumable. Moreover, the breath detection method used involves contact measurement, which may cause hygiene concerns. To achieve more convenient and accurate detection, many researchers have proposed methods to replace the traditional breath-type measurement instruments. The present study proposes a two-stage neural network for recognition of drunk driving: the first stage uses the simplified VGG network to determine the age range of the subject, and the second stage uses the simplified Dense-Net to identify the facial features of drunk driving. The age discrimination stage obtained an accuracy of 86.36%. In addition, in drunk driving recognition tests among various age groups (18–30, 31–50, and $\geq$51 years), accuracies of 94%, 83%, and 81% were obtained, respectively. The overall system also showed a high accuracy of 89.62% and 87.44%, which proves the robustness of the system while supporting its practical application.

**INDEX TERMS** Alcohol test, artificial intelligence, convolutional neural networks, deep neural networks, drunk driving detection.

## I. INTRODUCTION

Drunk driving is a severe problem in most countries around the world, and the governments of all countries have established punishments and methods to prevent drunk driving activities, including increasing penalties for driving under the influence, joint penalties for passengers, revocation of driving license, and imprisonment, among others. According to national statistics [1], although there is a downward trend in incidents of drunk driving accidents year on year, the results are still limited, and the suggested measured have not completely discouraged drunk driving.

Breath-alcohol meters are still mainly used as the means to detect drunk driving status; however, there are several problems with such an exhalate detection method, including the high price of the instrument, the mouthpiece is a consumable, which is not environmentally friendly, hygiene

The associate editor coordinating the review of this manuscript and approving it for publication was Fan Zhang[ID].

concerns, and inconvenient usage. Further, misjudgments are easily possible with the results owing to residual moisture in the instrument under continuous use conditions.

To replace the traditional breath-type measurement instruments, there were researches using thermal infrared images [2], 3-layered neural network [3], or weighted kernel based on electrocardiogram [4], to detect drunk driving. Recent studies have shown that deep neural networks (DNN), such as convolutional neural network (CNN) [5], visual geometry group (VGG) [6], dense convolutional network (Dense-Net) [7]–[9], and recurrent neural network (RNN) [10], can achieve a relatively accurate results for various applications. Therefore, several studies employed DNN to identify drunk person [11], [12]. Using a CNN to extract features and classifying it with RNN performs well on drunk person identification [11]. Since the alcohol test results may be affected by differences in age [12], the drunk driving recognition system proposed in this paper uses a two-stage neural network to first recognize the age and then drunk

# Compensator-Free Li-Ion Battery Charger with Current Window Control

Robert Chen-Hao CHANG[†a)], *Member*, Wei-Chih CHEN[†], *and* Shao-Che SU[†], *Nonmembers*

**SUMMARY**    A switching-based Li-ion battery charger without any additional compensation circuit is proposed. The proposed charger adopts a dual–current sensor and a current window control to ensure system stability in different charge modes: trickle current, constant current, and constant voltage. The proposed Li-ion battery charger has less chip area and a simpler structure to design than a conventional Li-ion battery charger with pulse width modulation. Simulation with a $1000\mu F$ capacitor as the battery equivalent, a 5V input, and a 1A charge current resulted in a charging time of 1.47ms and a 91% power efficiency.
*key words:* *switching-based, Li-ion battery, charger, compensation circuit*

## 1. Introduction

In recent years, Li-ion batteries have been widely used in electronic products such as digital cameras, notebook computers, smartphones, and tablets because they have high power density, long life, and high voltage [1]. Higher capacity Li-ion batteries are required to extend these products' usage time, but their longer charging time affects their convenience. Li-ion battery chargers commonly use two different structures: linear–regulator–based or switching-based [2]–[4]. A linear–regulator–based charger has the advantage of simple structure and negligible voltage ripple, but its power efficiency is affected by a large charge current and dropout voltage between the input and output voltages. In comparison, a switching–based charger has high power efficiency with large charge current and wide voltage range (input and output), but it requires additional off-chip components that increase cost [3]–[7]. The conventional switching-based charger usually adopts pulse-width modulation (PWM) to control the charge current in its trickle current (TC), constant current (CC), and constant voltage (CV) modes. Figure 1 shows the waveforms of charge current and battery voltage. However, PWM requires an additional compensation circuit to ensure system stability, increasing the PCB area and cost. Moreover, the additional compensation circuit is hard to design because of the charger's three charge modes.

In this letter, a switching-based compensator-free Li-ion battery charger is proposed that uses current window control to ensure system stability in all the charge modes. As the battery voltage increases, the proposed charger
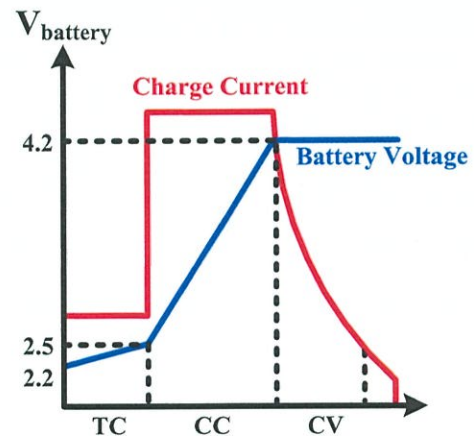
Fig. 1    Waveforms of battery voltage and charge current.

adaptively changes the charge current to switch between the TC, CC, and CV modes. The charger incorporates a comparator to generate a feedback loop; this has a simple structure and no additional compensation circuit, decreasing the chip area and cost.

## 2. Compensator-Free Li-Ion Battery Charger and Operating Principles

Figure 2 shows the proposed Li-ion battery charger schematic with its mode selector and current window controller. The mode selector detects the battery voltage and generates the current window control signal to switch the charge current level in the TC, CC, and CV modes. The current window control limits the charge current peak and valley values to ensure system stability. Furthermore, the feedback loop adopts a comparator to reduce chip area and cost as mentioned above. The key waveforms of the proposed charger are shown in Fig. 3. The operating principles of the TC, CC, and CV modes are as follows:

TC Mode ($t_0$–$t_1$): In this mode, the mode selector compares the feedback voltage $V_{fb}$ with the reference voltage $V_{ref\_tc}$ and maintains the control signal $V_{tc}$ at a value of 1 while the battery voltage is lower than 2.5V. The current window control limits the peak and valley value of charge current with reference voltages $V_{peak\_tc}$ and $V_{valley\_tc}$.

CC Mode ($t_1$–$t_2$): After the battery voltage becomes equal to or greater than 2.5V, the mode selector changes $V_{tc}$ to 0 and $V_{cc}$ to 1 to switch to CC mode. The

# A 93.4% Efficiency 8-mV Offset Voltage Constant On-Time Buck Converter With an Offset Cancellation Technique

Robert Chen-Hao Chang [ID], Wei-Chih Chen [ID], and Jerry Kuei-Shou Huang

*Abstract*—In this brief a constant on–time (COT) buck converter with high efficiency and low offset voltage is presented. It was fabricated with a TSMC 0.18$\mu$m 1P6M CMOS process. An additional current feedback path (ACFP) technique was incorporated to avoid subharmonic oscillation of the converter without a large equivalent series resistance (ESR) capacitor, thus reducing the output voltage ripple. However, the ACFP causes an offset voltage on the converter's output voltage dc level with loading changes. The proposed offset cancellation can remove the dc level from current sensor in ACFP. Hence, the offset voltage can be reduced through a proposed offset cancellation technique. The experimental results revealed that the offset voltage of the proposed converter is 8mV under a 0.1A to 1A loading changes. The converter's maximum power efficiency is 93.4 %, and its output voltage ripple is less than 18mV.

*Index Terms*—Constant on–time (COT), buck converter, additional current feed–back (ACFP), subharmonic oscillation, offset cancellation.

## I. INTRODUCTION

INTEGRATED power converter is an indispensable block in electronic products such as smart phones, tablets, and digital cameras, and even environmental sensors for the Internet of Things (IoT) applications that add convenience to human life. A battery is used to supply the power for these products, so the products enter standby mode when not operating to extend battery life. Thus, high power efficiency under a wide loading range is a critical power converter requirement. Pulse width modulation (PWM) control has high power efficiency under heavy loading, but high switching frequency cause large switching loss, degrading converter power efficiency under light loading condition. In order to improve the power efficiency, a dual mode control implemented with pulse frequency modulation and pulse width modulation (PFM/PWM) control has been proposed. PFM control is used to reduce switching loss by operating in discontinuous conduction mode (DCM) to improve the power efficiency under light loading [1]–[2].

In addition, PWM is applied to obtain high power efficiency under heavy loading. Thus, high power efficiency of the power converter is achieved under both light and heavy loading. On the other hand, dual mode control requires two modulation controllers (PFM/PWM) which use complex control circuit and occupy more chip area.

The ripple–based constant on–time (COT) control technique has received more attention in recent years because of its simple architecture and high power efficiency under a wide loading range [3]–[5]. For light loading, COT converter improves power efficiency by means of its variable switching frequency and DCM operation, resulting in low switching loss. When COT converter operated with heavy loading, it uses continuous conduction mode (CCM) control to reduce conduction loss, thus obtaining high power efficiency. However, conventional COT converter requires a large capacitor equivalent series resistance (ESR) to provide sufficient inductor current information to avoid instability when it operates in CCM. In order to ensure stability, the $R_{ESR}$ multiplied by output capacitor $C_O$ is required to be larger than half the time of power MOS turn-on [6]–[8]. Furthermore, a large value of ESR causes higher output ripple voltage and decreases the power efficiency of conventional COT converter under heavy loading. Multilayer ceramic capacitor (MLCC) has a small ESR and size, which if adopted in a conventional COT converter provides reduced output ripple, high power efficiency, and reduced PCB area, but causes instability. To decouple inductor current information from ESR, the ACFP technique was proposed [9]–[12]. By using a current sensor to sense the inductor information and inject it into the feedback loop, the instability issue is resolved for COT converter with a small ESR capacitor. However, the ACFP technique generates an offset voltage on the output voltage dc level of the power converter when the loading changes, thus affecting the power converter's accuracy [9].

This brief proposes a constant on-time buck converter with an additional feedback current path (ACFP) and offset cancellation technique. The ACFP technique is incorporated to overcome the instability due to a small ESR capacitor. The offset cancellation technique is proposed to reduce the converter output offset voltage for loading changes. Moreover, the proposed offset cancellation technique employs three differential pairs instead of the conventional voltage to current converter (V–I converter) which improve power efficiency and reduce the chip area. The proposed COT buck converter chip

# An AC–DC Rectifier With Active and Non-Overlapping Control for Piezoelectric Vibration Energy Harvesting

Robert Chen-Hao Chang[ID], Wei-Chih Chen, Lin Liu, and Sheng-Hung Cheng

*Abstract*—This brief presents an ac–dc rectifier for piezoelectric vibration energy harvesting application. The proposed rectifier is designed and implemented with TSMC 0.25 $\mu$m 1P3M 5-V CMOS process. Active control is proposed to eliminate the voltage drop from the traditional diode forward voltage and the reverse current from the output capacitor to input source. The simultaneously turn on and oscillation on power MOS $M_{N1} - M_{N2}$ gate signal $V_{GN1} - V_{GN2}$ has been overcome by a 40-ns delay time which generated by a non-overlapping control. The experimental results indicated maximum power efficiency 95% and voltage conversion ratio 99% are achieved at 20 k$\Omega$ and 200 k$\Omega$ loading resistor.

*Index Terms*—Active control, non-overlapping control, piezo-electric vibration energy harvesting, rectifier.

## I. INTRODUCTION

IN RECENT years, rechargeable batteries have been widely used as a power supply for microchip devices such as environmental sensors and biomedical devices, for which the usage time is limited by the energy of the battery. A major problem with these devices is that battery required recharging or replacement. An efficient energy harvesting system is the solution to this problem. Solar, vibration, thermal, and RF energy are common sources of energy harvesting. However, solar and thermal energy are unsuitable power sources for the microchip device application, because of the lack of sunlight and temperature at all time. Moreover, RF energy mainly scavenges radio waves form the surrounding antennas or base stations. Vibration energy is a suitable power source for microchip applications because it has high output voltage amplitude. Because the output of vibration energy harvester is an ac voltage, an ac–dc rectifier is required to generate a usable dc output power. Several studies [1]–[12] have focused on improving the power efficiency and voltage conversion ratio in this scenario. The conventional rectifiers use diode switches [1]–[3] to rectify the ac input voltage to dc output

voltage. However, the diode forward voltage drop reduces the power efficiency and voltage conversion ratio. Studies [4]–[12] have proposed using the power MOS instead of the diodes. In the rectifier operation, the output voltage is nearly identical to the input amplitude because of the power MOS function as an active diode [7]–[12], exhibiting the ideal diode characteristic of a voltage drop approaching zero. A small voltage drop improving the rectifier power efficiency and voltage conversion ratio.

A small voltage drop during the MOS switch turn on in an active n-type MOS (NMOS) cross-coupled p-type MOS (PMOS) improves the power efficiency and voltage conversion ratio of the rectifier in [7] and [8]. Guo and Lee [7] use the unbalanced comparator to generate an offset voltage to eliminate the reverse current when the output voltage is higher than the input amplitude. However, the offset voltage of the unbalanced comparator suffers in process variation and affects the operation of the rectifier. The offset voltage with process variation may cause oscillations [8] that affect the stability of the rectifier and decrease the power efficiency. Chang *et al.* [12] proposed fully active control using active NMOS and active PMOS to ensure that the reverse current through the PMOS to the input source is zero. However, the two active NMOS devices may turn on at the same time and cause the power loss at input source. Wu *et al.* [11] discussed the Synchronized Switch Harvesting on Inductor SSHI and Synchronous Electrical Charge Extraction SECE, which extracts more energy from the piezoelectric model. Both SSHI and SECE have an external switch and inductor that form an LC resonant circuit for oscillation, which transfer the energy to an output capacitor and a loading when the input amplitude is at its peak. However, external components and complex control circuits are required to ensure that the switch is turned on at an appropriate time, thus increasing the cost of the chip.

In this brief, a rectifier with active and non-overlapping control is proposed that overcomes the previously discussed unwanted operation of the rectifier. The proposed rectifier uses two active PMOS and two NMOS devices; the unbalanced comparator $comp_1 - comp_2$ to accurately detect the input source with output voltage to avoid the reverse current, and the comparator $comp_3$ to detect the input source under the positive or negative cycle to eliminate the oscillation of the NMOS. The logic gate generates a non-overlapping control signal of the NMOS devices to ensure the rectification without the simultaneous turn on of the two power NMOS devices.

# A 17.5-to-21-GHz Current-Folding Frequency Tripler With >36-dBc Harmonic Rejection in 90-nm CMOS

Ching-Yuan Yang , *Member, IEEE*, Chun-Hung Lin, Robert Chen-Hao Chang , *Senior Member, IEEE*, and Samuel Palermo , *Senior Member, IEEE*

*Abstract*—In this letter, a current-folding frequency tripler (FT) is presented to convert the fundamental input into the triple-frequency output. To demonstrate FT operation, we built in a voltage-controlled oscillator (VCO) to generate the fundamental signal and used a band-pass stage for harmonic suppression. Fabricated in the 90-nm CMOS technology, the core consumes 5 mW from 1.2-V supply. When the measured tuning range of VCO is from 5.83 to 7 GHz, the FT features 36 to 43-dBc fundamental harmonic rejection from 17.5 to 21 GHz. The phase noise of the FT at 18.96 GHz is −102.8 dBc/Hz at 1-MHz offset while the VCO is with −112.5 dBc/Hz.

*Index Terms*—Current-folding, frequency tripler (FT), fundamental harmonic rejection, voltage-controlled oscillator (VCO).

## I. INTRODUCTION

At microwaves and millimeter-waves, a frequency tripler (FT) after the voltage-controlled oscillator (VCO) allows the synthesizer to have a lower RF division ratio and allows the VCO to run at one-third the frequency. The benefit is that there is no need to use a high-frequency fundamental oscillator with poor phase noise (PN), limited tuning range, and high-power consumption in CMOS processes. On the contrary, these factors reduce LO PN, ideally offsetting the 9.54-dB noise penalty incurred by using an FT. FTs can be categorized in three main groups: 1) multiphase combiner based; 2) mixer based; and 3) third harmonic extractor based. Combining multiphase input signals is a simple FT approach remove all but the desired harmonics, but its harmonic suppression depends on the precision of phase shift progress between polyphase input signals [1]. For self-mixing FT approaches, as the VCO exhibits the fundamental and second-order harmonic components, we can use self-mixing to produce the desired triple-frequency output from a bandpass filter (BPF). The self-mixing approach seems simple, but it has limited suppression of harmonics, especially signal components at two input frequencies [2], [3], [4], [5], [6]. An alternative to generate the desired output signal of FT is to overdrive the amplifier and exploit its harmonic distortion [7], [8], [9]. For example, the techniques employing the third harmonic extraction with clips or deep cuts [8] from the nonlinear combiner were proposed to generate the third harmonic frequency output. However, their conversion efficiency is generally limited by the intrinsic overdriven techniques.

In this letter, a new FT directly converts the fundamental input into the triple-frequency output via a fully differential current-folding stage with inherent third-harmonic enhancement [10]. Unlike self-mixing or polyphase-edge combining techniques, in this letter the proposed folding architecture can reduce hardware to performs FT
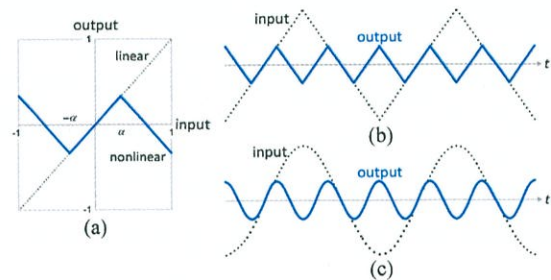
Fig. 1. Basic concepts: (a) transfer curve of proposed folding FT, (b) FT operation with the input triangle wave, and (c) ideal third harmonic enhancement for sinusoidal waveforms.

preprocessing. A built-in VCO is used as the fundamental generator, and the proposed current-folding stage converts the fundamental input to the tripled output, which is then injected into a bandpass stage for harmonic suppression.

## II. THIRD-HARMONIC ENHANCEMENT WITH FOLDING TRANSFER

### A. Third-Harmonic Enhancement

The proposed FT adopts a current-folding technique to achieve inherently nonlinear operation to enhance the third harmonic signals. Fig. 1(a) shows the simple concept of our proposal FT-normalized nonlinear transfer curve, including twofold points at $\pm\alpha$. The FT performs two matching fold points for input–output characteristic, featured by the triangular shape. The folding configuration generates output node matched at the third harmonic frequency. In Fig. 1(b), the folding mechanism converts the input triangle wave into a tripled output waveform. As shown in Fig. 1(c), we expect the fundamental sinusoidal waveforms to collapse into their shape, resulting in a significant enhancement of the third harmonic signal. Instead, the fundamental wave is reduced, and ideally can be completely removed, leaving only the third harmonic signal. As a result, the requirement for on-chip high-$Q$ filters can be alleviated using the enhanced third harmonic technique. A simple on-chip $LC$ BPF is used for effective harmonic suppression. The FT adopting the proposed folding approach easily overcome limitations of conventional polyphase-edge combining or self-mixing techniques, because only one fundamental input path is considered and it still retains the original advantage.

Without using the BPF stage, we directly utilize an ideal FT transfer curve to convert the fundamental sine wave to a folding waveform. Fig. 2(a) shows the nonlinear FT transfer-function-based generation, where the folding voltage is $V_F$. MATLAB simulation was performed to verify the folding conversion. The fundament sinusoidal input has the swing of $\pm V_{SW}$ at $\omega_0$. Analyzing the folding output in terms of FFT, we can really find that it is feasible to implement FT using the folding technique. As the folding voltage is varied, Fig. 2(b) shows the fundamental (HRR31) and fifth-order (HRR35) harmonic rejection performances. Obviously, the quality of tripled output depends on its folding voltage. Since HRR35 is low enough compared to HRR31, it will not be discussed later. The proposed FT can achieve the highest HRR31 as the folding voltage is set to around $0.4V_{SW}$.

# Design and Implementation of LoRa-Based Wireless Sensor Network with Embedded System for Smart Agricultural Recycling Rapid Processing Factory

Chia-Yu WANG[†], Chia-Hsin TSAI[†], Sheng-Chung WANG[†], Chih-Yu WEN[†], *Nonmembers*, Robert Chen-Hao CHANG[†], *and* Chih-Peng FAN[†a)], *Members*

**SUMMARY**    In this paper, the effective Long Range (LoRa) based wireless sensor network is designed and implemented to provide the remote data sensing functions for the planned smart agricultural recycling rapid processing factory. The proposed wireless sensor network transmits the sensing data from various sensors, which measure the values of moisture, viscosity, pH, and electrical conductivity of agricultural organic wastes for the production and circulation of organic fertilizers. In the proposed wireless sensor network design, the LoRa transceiver module is used to provide data transmission functions at the sensor node, and the embedded platform by Raspberry Pi module is applied to support the gateway function. To design the cloud data server, the MySQL methodology is applied for the database management system with Apache software. The proposed wireless sensor network for data communication between the sensor node and the gateway supports a simple one-way data transmission scheme and three half-duplex two-way data communication schemes. By experiments, for the one-way data transmission scheme under the condition of sending one packet data every five seconds, the packet data loss rate approaches 0% when 1000 packet data is transmitted. For the proposed two-way data communication schemes, under the condition of sending one packet data every thirty seconds, the average packet data loss rates without and with the data-received confirmation at the gateway side can be 3.7% and 0%, respectively.
*key words:  IoT, LoRa, wireless sensor network, smart manufacture for smart agriculture, embedded system*

## 1. Introduction

Development of agriculture is one of the most important parts for any country's economic requirement, and the Internet of Things (IoT) based network, which is composed of various sensor nodes for monitoring soil acidity, temperature, and other variables, has been broadly adopted for the smart-manufacturing based agriculture related fields. In [1], to control food quality and quantity, the IoT and sensor node based technologies were beneficial to promote smart agriculture, urban farming, agriculture robots, automation, and future food expectation, etc. In [2], the researchers developed a smart agriculture system which utilizes Arduino, IoT, and wireless sensor network to improve yield of the efficient crops. The system had a duplex communication link by a cellular-Internet interface that permit for data

inspection and irrigation scheduling. In [3], the design included smart GPS based remote controlled robot to perform many agriculture tasks, and all of the operations were connected by the sensor modules, the Wi-Fi/ZigBee modules, the actuators combined with the Micro Control Unit (MCU) and Raspberry Pi platform. In [4], the system was developed with many sensor nodes based components, which included water level, soil moisture, temperature, humidity, and rain sensors, and the LoRa based technology is used for the data transmission module. In [5], the IoT based technology supported crop management, resource management, crop monitoring and field monitoring, etc. The IoT based sensors used in proposed design were temperature sensor, soil pH sensor, soil moisture sensor, humidity sensor, water volume sensor, etc.

Besides, the smart manufacturing technologies combined with IoT and big data analysis were applied to improve the production performance of smart agriculture related domains. In [6], the researchers reviewed the IoT related technologies and systems which are the foundations of data-driven innovations for smart manufacturing, and the evolution of IoT based networks connected many manufacturing things, which included materials, sensors, equipment, people, products, and supply chain to emerge the effective cloud computing architecture. The time-sensitive properties of sensing data generated the challenges of the real-time collection, processing, and decision making. In [7], the proposed design described how the adoption of IoT in manufacturing by considering sensor based systems and mobile devices to generate industrial big data. In [8], the effective and smart factory solution was proposed to verify the real factory environment by the NB-IoT based network to get the economical implementation. For the smart agriculture related applications, in [9], the effective IoT applications with the LoRa based wireless sensor network designs were introduced, and the IoT technology was utilized to monitor the condition of air quality levels, which contains temperature, air humidity, CO, and CO2. The system used ATmega328P-AU as a controller, and employed the LoRa module for data transmission, and applied Antares to be a cloud service for data storage. In [10], the real-time LoRa based standalone air quality monitoring system was developed to remotely measure PM 2.5, carbon monoxide, carbon dioxide, temperature, humidity, and air pressure. The data from different

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# The role of government policy in the building of a global semiconductor industry

With careful planning and a focus on developing expertise, government policy has helped Taiwan become a centre for semiconductor innovation.

Meng-Fan Chang, Ching Lin, Chang Hong Shen, Sung Wen Wang, Kuo Cheng Chang, Robert Chen-Hao Chang and Wen Kuan Yeh

Forty years after adopting rudimentary technology from the US, Taiwan now holds a 30% market share of the world's semiconductor industry. It leads the world in semiconductor foundries and integrated circuit (IC) packaging and testing with a global market share of more than 70% and 50%, respectively, and is ranked second only to the US in chip design with a global market share of more than 18%. Its science parks support a complete semiconductor industry, from IC design to manufacturing, packaging and testing, as well as the supporting industries that produce wafers, masks and chemicals. And it is home to the world's largest semiconductor foundry, Taiwan Semiconductor Manufacturing Company (TSMC), and the largest IC packaging and testing firm, Advanced Semiconductor Engineering, Inc. (ASE).

The success of Taiwan's semiconductor industry can be largely attributed to ongoing investment in research and development at the industry level, and the government's unwavering commitment to cultivating engineering skills and talent. These accomplishments can be traced back to the Integrated Circuit Project that was initiated by the government of Taiwan in 1974 (Table 1). The project established a foundation for the development of the semiconductor industry and the reshaping of the broader economy.

## The foundations for development (1974–1979)

In the 1970s, much of the world was experiencing economic recession and inflation, and Taiwan was importing nearly all of the IC chips used in its growing electronics industry. However, the government recognized this as an opportunity to transform and accelerate Taiwan's industry. In 1974, the minister of economic affairs, Yun-Suan Sun, looked to bypass cumbersome government channels and to develop and recruit electronic engineering talent by establishing the Electronics Industrial Research Centre (later known as the Electronics Research and Service Organization (ERSO)) of the Industrial Technology Research Institute (ITRI).

ITRI-ERSO played a crucial role in developing semiconductor technologies between 1976 and 1979 when it implemented phase I of the publicly funded Electronics Industry Development Project (EIDP; Table 1). In March 1976, ITRI-ERSO signed a 10-year contract with the US manufacturer Radio Corporation of America (RCA) to acquire semiconductor technologies, and by the following month, ITRI-ERSO was sending personnel to RCA for training. Just three months later, a ceremony was held for the opening of the first IC demonstration plant at ITRI, which in the fall of 1977 produced Taiwan's first 3-inch silicon wafer. Despite these critical early advances in developing a domestic semiconductor industry, private enterprise did not initially share the government's enthusiasm, preferring to limit investment to IC packaging for foreign firms such as Philips, Texas Instruments and Motorola.

## Nurturing semiconductor companies (1979–1989)

Phase II of the EIDP was implemented between 1979 and 1983 (Table 1). The Taiwanese government established the Hsinchu Science Park, which became known as the Silicon Valley of the East[1], in 1980. A corporate spin-off of ERSO — United Microelectronics Corporation (UMC) — was then created in 1980. This was jointly funded by the government and a number of investors, and marked the starting point of semiconductor manufacturing in Taiwan.

In 1983, the government sponsored phase III of the EIDP in response to the development of very-large-scale integration (VLSI) technologies, which was being driven by leading overseas firms. The resulting VLSI Circuit Technology Development Project (1983–1988) was given a budget of approximately US$74.5 million and a specific agenda to develop in-house IC technology know-how, a complete IC supply chain, and a support centre for the domestic electronics industry. Over the course of this project, ITRI-ERSO oversaw the transfer of leading technologies, including 1.25-μm complementary metal–oxide–semiconductor (CMOS) manufacturing from the US company Vitelic Technology. Researchers at ITRI-ERSO also developed proprietary 1.5-μm 256-K CMOS dynamic random-access memory (DRAM) technology.

In 1987, TSMC was spun off from ITRI using capital from the government, private investors and Philips Inc. Crucially, the foundry services provided by TSMC freed IC design houses from the burden of investing in expensive manufacturing facilities and helped to stimulate faster growth in the global IC design industry. In the same year, a number of companies established facilities in the Hsinchu Science Park, including Mosel Vitelic Inc., the Hualon Microelectronics Corporation and the Winbond Electronics Corporation. By the end of this period, there were 25 domestic IC design houses and 8 semiconductor manufacturing companies operating in Taiwan.

## Handing off control (1989–2000)

Beginning in the early 1990s, the government gradually changed its support strategy for the semiconductor industry from government oversight and subsidization to tax incentives and investment. The 5-year Development Project of Submicron Manufacturing Process Technology was launched in 1990 with a budget of US$280 million. Organizers in the Ministry of Economic Affairs put together an alliance comprising UMC, TSMC, Winbond Electronics Corporation, Mosel Vitelic, Macronix International Co. (MXIC) and Advanced Microelectronic Products, Inc. Companies providing supply

張振豪

## 112年度 【 應用於生理感測之高解析度雜訊整形逐次逼近類比數位轉換器 】經費核定清單

執行機構：國立中興大學　　　　　　　　主　持　人：張振豪　　教授[電機工程學系（所）]

| 補助項目 | 申請金額 | 核定金額 | 說　　　　　明 |
|---|---|---|---|
| 業務費 | 750,000 | 412,000 | 一、研究人力、耗材、物品、圖書及雜項等費用<br>※計畫主持人得依執行機構自訂標準考量實際約用研究人力之工作內容、專業技能、預期績效表現等因素，於補助經費內調整核給相關費用，但不得低於本會規定最低標準。<br>二、本計畫彈性支用額度為12,960元 |
| 研究設備費 | 195,000 | 100,000 | 低雜訊差動感測器 |
| 國外差旅費 | 100,000 | 60,000 | 一、出席國際學術會議：60,000元<br>二、本項目不核列管理費 |
| 管理費 | 141,750 | 76,000 | |
| 合　　　計 | 1,186,750 | 648,000 | 執行期限：　112/08/01 ～ 113/07/31<br>計畫編號：　NSTC 112-2221-E-005-097 - |

研究類型：一般研究計畫(個別型)
學門名稱：積體電路及系統設計
應繳報告：成果報告
研究成果歸屬：國立中興大學
流水號：112WFA0510357
承辦人：潘敏治
聯絡電話：02-2737-7983

各項費用之支用請依「國家科學及技術委員會補助專題研究計畫經費處理原則」規定辦理。
年度所需經費如未獲立法院審議通過或經部分刪減，國家科學及技術委員會得依審議結果調減補助經費，並按預算法第五十四條規定辦理。
如未依規定繳交報告或執行成效未如預期且計畫主持人未盡力改善時，國家科學及技術委員會得調減次年度經費或終止執行該計畫。

## 112年度 【 應用於第六代通訊之小晶片異質整合的每秒兆位元全雙工收發器(2/4) 】經費核定清單

執行機構：國立中興大學　　　　　　　　主　持　人：張振豪　　教授[電機工程學系（所）]
　　　　　　　　　　　　　　　　　　　共同主持人：林泓均　　教授[電機工程學系（所）]
　　　　　　　　　　　　　　　　　　　　　　　　　楊清淵　　教授[電機工程學系（所）]
　　　　　　　　　　　　　　　　　　　　　　　　　許恒銘　　教授[電機工程學系（所）]
　　　　　　　　　　　　　　　　　　　　　　　　　江衍忠　　副教授[電機工程學系（所）]
　　　　　　　　　　　　　　　　　　　　　　　　　黃穎聰　　教授[電機工程學系（所）]

| 補助項目 | 申請金額 | 核定金額 | 說　　　　　明 |
|---|---|---|---|
| 業務費 | 5,501,856 | 4,301,800 | 一、研究人力、耗材、物品、圖書及雜項等費用<br>1.本會依規定主動增核研究主持費1名，月支15,000元(12.00月計)<br>※計畫主持人得依執行機構自訂標準考量實際約用研究人力之工作內容、專業技能、預期績效表現等因素，於補助經費內調整核給相關費用，但不得低於本會規定最低標準。<br>二、本計畫彈性支用額度為25,000元 |
| 研究設備費 | 4,968,000 | 3,000,000 | FPGA 開發板，個人電腦，向量網路分析儀，任意波形產生器系統升級，數位通訊分析儀，工作站，雷射印表機 |
| 國外差旅費 | 600,000 | 480,000 | 一、出席國際學術會議：480,000元<br>二、本項目不核列管理費 |
| 管理費 | 925,278 | 718,200 | 研究主持費不核列管理費 |
| 合　　　計 | 11,995,134 | 8,500,000 | 執行期限：　112/05/01 ～ 113/04/30<br>計畫編號：　NSTC 112-2218-E-005-006 - |

研究類型：一般策略專案計畫(整合型)
學門名稱：通訊晶片
多年期計畫
流水號：112PFA0510715
承辦人：潘敏治
聯絡電話：02-2737-7983

應繳報告：期中報告(請於計畫執行期滿前二個月，至本會網站線上繳交進度報告，以憑核定下年度經費)
研究成果歸屬：國立中興大學
各項費用之支用請依「國家科學及技術委員會補助專題研究計畫經費處理原則」規定辦理。

111年度【 應用於第六代通訊之小晶片異質整合的每秒兆位元全雙工收發器(1/4)】經費核定清單

執行機構：國立中興大學

主　持　人：張振豪　　教授[電機工程學系（所）]
共同主持人：林泓均　　教授[電機工程學系（所）]
　　　　　　楊清淵　　教授[電機工程學系（所）]
　　　　　　許恒銘　　教授[電機工程學系（所）]
　　　　　　江衍忠　　副教授[電機工程學系（所）]
　　　　　　黃穎聰　　教授[電機工程學系（所）]

| 補助項目 | 申請金額 | 核定金額 | 說　　　　明 |
|---|---|---|---|
| 業務費 | 5,501,856 | 4,530,800 | 一、研究人力、耗材、物品、圖書及雜項等費用<br>　1.本部依規定主動增核研究主持費(111/8~112/4)1名，月支15,000元(9.00月計)<br>※計畫主持人得依執行機構自訂標準考量實際約用研究人力之工作內容、專業技能、預期績效表現等因素，於補助經費內調整核給相關費用，但不得低於本部規定最低標準。<br>二、本計畫彈性支用額度為25,000元 |
| 研究設備費 | 4,958,000 | 4,000,000 | FPGA 開發板，個人電腦，筆記型電腦，雷射印表機，不斷電系統，工作站，資料儲存系統，任意波形產生器 |
| 國外差旅費 | 600,000 | 480,000 | 一、出席國際學術會議：480,000元<br>二、本項目不核列管理費 |
| 管理費 | 925,278 | 759,200 | 研究主持費不核列管理費 |

| 補助項目 | 申請金額 | 核定金額 | 說　　　　明 |
|---|---|---|---|
| 合　　計 | 11,985,134 | 9,770,000 | 執行期限： 111/05/01 ～ 112/04/30<br>計畫編號： MOST 111-2218-E-005-008 - |

研究類型：一般策略專案計畫(整合型)　　　　　　多年期計畫　　　　　　流水號：111WFA0510715
學門名稱：通訊晶片　　　　　　　　　　　　　　　　　　　　　　　　承辦人：潘敏治
　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　　聯絡電話：02-2737-7983

應繳報告：期中報告(請於計畫執行期滿前二個月，至本部網站線上繳交進度報告，以憑核定下年度經費)
研究成果歸屬：國立中興大學
各項費用之支用請依「科技部補助專題研究計畫經費處理原則」規定辦理。
年度所需經費如未獲立法院審議通過或經部分刪減，科技部得依審議結果調減補助經費，並按預算法第五十四條規定辦理。
如未依規定繳交報告或執行成效未如預期且計畫主持人未盡力改善時，科技部得調減次年度經費或終止執行該計畫。

## 110年度 【 低功率生理感測電路設計(II) 】經費核定清單

執行機構：國立中興大學

主　持　人：張振豪　　教授[電機工程學系（所）]
共同主持人：林泓均　　教授[電機工程學系（所）]
　　　　　　楊清淵　　教授[電機工程學系（所）]
　　　　　　江衍忠　　副教授[電機工程學系（所）]

| 補助項目 | 申請金額 | 核定金額 | 說　　　　明 |
|---|---|---|---|
| 業務費 | 1,817,856 | 930,000 | 一、研究人力、耗材、物品、圖書及雜項等費用<br>　1.本部依規定主動增核研究主持費1名，月支15,000元(12.00月計)<br>　※計畫主持人得依執行機構自訂標準考量實際約用研究人力之工作<br>　　內容、專業技能、預期績效表現等因素，於補助經費內調整核給<br>　　相關費用。<br>二、本計畫彈性支用額度為25,000元 |
| 研究設備費 | 1,375,727 | 200,000 | 電流量測系統 |
| 國外差旅費 | 100,000 | 80,000 | 一、出席國際學術會議：80,000元<br>二、本項目不核列管理費 |
| 管理費 | 372,678 | 142,000 | 研究主持費不核列管理費 |
| 合　　　計 | 3,666,261 | 1,352,000 | 執行期限：110/08/01 ～ 111/07/31<br>計畫編號： MOST 110-2221-E-005-085 - |

研究類型：一般研究計畫(個別型)
學門名稱：積體電路及系統設計
應繳報告：成果報告
研究成果歸屬：國立中興大學
各項費用之支用請依「科技部補助專題研究計畫經費處理原則」規定辦理。
年度所需經費如未獲立法院審議通過或經部分刪減，科技部得依審議結果調減補助經費，並按預算法第五十四條規定辦理。
如未依規定繳交報告或執行成效未如預期且計畫主持人未盡力改善時，科技部得調減次年度經費或終止執行該計畫。

流水號：110WFA0510231
承辦人：潘敏治
聯絡電話：02-2737-7983

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## 109年度 【 無線低功率安全偵測單晶片系統設計－總計畫暨子計畫一：低功率生理感測電路設計 】經費核定清單

執行機構：國立中興大學

主　持　人：張振豪　　教授[電機工程學系（所）]
共同主持人：楊清淵　　教授[電機工程學系（所）]
　　　　　　林泓均　　教授[電機工程學系（所）]
　　　　　　江衍忠　　副教授[電機工程學系（所）]

| 補助項目 | 申請金額 | 核定金額 | 說　　　　明 |
|---|---|---|---|
| 業務費 | 1,433,856 | 1,425,800 | 一、研究人力、耗材、物品、圖書及雜項等費用<br>　1.本部依規定主動增核研究主持費1名，月支15,000元(12.00月計)<br>　※計畫主持人得依執行機構自訂標準考量實際約用研究人力之工作<br>　　內容、專業技能、預期績效表現等因素，於補助經費內調整核給<br>　　相關費用。<br>二、本計畫彈性支用額度為25,000元 |
| 研究設備費 | 1,158,331 | 750,000 | 元件電流波形分析儀，雙通道電流感測器 |
| 國外差旅費 | 100,000 | 100,000 | 一、出席國際學術會議：100,000元<br>二、本項目不核列管理費 |
| 管理費 | 315,078 | 286,200 | 研究主持費不核列管理費 |
| 合　　　計 | 3,007,265 | 2,562,000 | 執行期限：109/08/01 ～ 110/07/31<br>計畫編號： MOST 109-2221-E-005-048 - |

研究類型：一般研究計畫(整合型)
學門名稱：積體電路及系統設計
應繳報告：成果報告
研究成果歸屬：國立中興大學
各項費用之支用請依「科技部補助專題研究計畫經費處理原則」規定辦理。
年度所需經費如未獲立法院審議通過或經部分刪減，科技部得依審議結果調減補助經費，並按預算法第五十四條規定辦理。
如未依規定繳交報告或執行成效未如預期且計畫主持人未盡力改善時，科技部得調減次年度經費或終止執行該計畫。

流水號：109WFA0510381
承辦人：潘敏治

108年度 【 人工智慧監控與辨識系統:應用於身份辨識之低功率深度學習可重組加速器晶片－人工智慧監控與辨識系統:應用於身份辨識之低功率深度學習可重組加速器晶片(3/3) 】經費核定清單

執行機構：國立中興大學　　　　　　　主　持　人：張振豪　　教授[電機工程學系（所）]
　　　　　　　　　　　　　　　　　　共同主持人：賴永康　　教授[電機工程學系（所）]
　　　　　　　　　　　　　　　　　　　　　　　　吳崇賓　　助理教授[電機工程學系（所）]
　　　　　　　　　　　　　　　　　　　　　　　　范志鵬　　教授[電機工程學系（所）]

| 補助項目 | 申請金額 | 核定金額 | 說　　　　明 |
|---|---|---|---|
| 業務費 | 3,770,764 | 2,608,700 | 一、研究人力、耗材、物品、圖書及雜項等費用<br>※計畫主持人得依執行機構自訂標準考量實際約用研究人力之工作內容、專業技能、預期績效表現等因素，於補助經費內調整核給相關費用。<br>二、本計畫彈性支用額度為25,000元 |
| 研究設備費 | 2,748,000 | 1,000,000 | SOC設計平台，高速運算伺服器，ARM模擬驗證平台，晶片設計工作站，行動驗證裝置，電腦週邊設備，取像攝影機，掃描設備，雲端計算伺服器 |
| 國外差旅費 | 400,000 | 400,000 | 一、出席國際學術會議：400,000元<br>二、本項目不核列管理費 |
| 管理費 | 665,615 | 491,300 | |
| 合　　　計 | 7,584,379 | 4,500,000 | 執行期限：　108/06/01 ～ 109/05/31<br>計畫編號：MOST 108-2218-E-005-017 - |

研究類型：一般研究計畫(整合型)
研究性質：技術發展
應繳報告：期末報告
研究成果歸屬：國立中興大學

多年期計畫 學門名稱：人工智慧(AI on chip)　流水號：108PFA0550661
　　　　　　　　　　　　　　　　　　　　承辦人： 張庭軒

各項費用之支用請依「科技部補助專題研究計畫經費處理原則」規定辦理。
各年度所需經費如未獲立法院審議通過或經部分刪減，科技部得依審議情形調減補助經費。
如未依規定繳交報告或執行成效未如預期且計畫主持人未盡力改善時，科技部得調減次年度經費或終止執行該計畫。

【 基於深度學習之手掌靜脈辨識及其硬體加速器之設計(2/2) 】第2年經費清單

執行機構：國立中興大學　　　　　　　主　持　人：張振豪　　教授[電機工程學系（所）]

| 補助項目 | 申請金額 | 核定金額 | 說　　　　明 |
|---|---|---|---|
| 業務費 | 606,000 | 684,000 | 一、研究人力、耗材、物品、圖書及雜項等費用<br>1.本部依規定主動增核研究主持費1名，月支15,000元(12.00月計)<br>※計畫主持人得依執行機構自訂標準考量實際約用研究人力之工作內容、專業技能、預期績效表現等因素，於補助經費內調整核給相關費用。<br>二、本計畫彈性支用額度為19,940元 |
| 研究設備費 | 175,000 | 120,000 | AI晶片設計工作站，FPGA發展板 |
| 國外差旅費 | 100,000 | 100,000 | 一、出席國際學術會議：100,000元<br>二、本項目不核列管理費 |
| 管理費 | 117,150 | 93,000 | 研究主持費不核列管理費 |
| 合　　　計 | 998,150 | 997,000 | |

執行期限：108/08/01 ～ 109/07/31　　　　計畫編號：MOST 107-2221-E-005 -060 -MY2

研究類型：一般研究計畫(個別型)

## 【 基於深度學習之手掌靜脈辨識及其硬體加速器之設計(1/2) 】第1年經費清單

執行機構：國立中興大學　　　　　　　主 持 人：張振豪　　教授[電機工程學系（所）]

| 補助項目 | 申請金額 | 核定金額 | 說　　　　明 |
|---|---|---|---|
| 業務費 | 606,000 | 684,000 | 一、研究人力、耗材、物品、圖書及雜項等費用<br>　1.本部依規定主動增核研究主持費1名，月支15,000元(12.00月計)<br>　※計畫主持人得依執行機構自訂標準考量實際約用研究人力之工作<br>　　內容、專業技能、預期績效表現等因素，於補助經費內調整核給<br>　　相關費用。<br>二、本計畫彈性支用額度為19,940元 |
| 研究設備費 | 175,000 | 120,000 | AI晶片設計工作站，FPGA發展板 |
| 國外差旅費 | 100,000 | 100,000 | 一、出席國際學術會議：100,000元<br>二、本項目不核列管理費 |
| 管理費 | 117,150 | 93,000 | 研究主持費不核列管理費 |
| 合　　計 | 998,150 | 997,000 | |

執行期限：107/08/01 ～ 109/07/31　　　　計畫編號：MOST 107-2221-E-005 -060 -MY2

研究類型：一般研究計畫(個別型)

## 107年度 【 人工智慧監控與辨識系統:應用於身份辨識之低功率深度學習可重組加速器晶片－人工智慧監控與辨識系統:應用於身份辨識之低功率深度學習可重組加速器晶片(2/3) 】經費核定清單

執行機構：國立中興大學　　　　　主 持 人：張振豪　　　教授[電機工程學系（所）]
　　　　　　　　　　　　　　　共同主持人：吳崇賓　　　助理教授[電機工程學系（所）]
　　　　　　　　　　　　　　　　　　　　范志鵬　　　教授[電機工程學系（所）]
　　　　　　　　　　　　　　　　　　　　賴永康　　　教授[電機工程學系（所）]

| 補助項目 | 申請金額 | 核定金額 | 說　　　　明 |
|---|---|---|---|
| 業務費 | 3,770,764 | 2,574,700 | 一、研究人力費：2,029,700元<br>　1.助理人員費用2,029,700元<br>二、耗材、物品、圖書及雜項費用：545,000元<br>三、本計畫彈性支用額度為25,000元 |
| 研究設備費 | 2,759,000 | 1,500,000 | 多核心晶片設計平台，FPGA雛型驗證平台，ARM模擬驗證平台，晶片設計工作站，行動驗證裝置，電腦週邊設備，取像攝影機，掃描設備，高階FPGA_SoC發展平台，中階FPGA_SoC發展平台 |
| 國外差旅費 | 400,000 | 400,000 | 一、出席國際學術會議：400,000元<br>二、本項目不核列管理費 |
| 管理費 | 665,615 | 485,300 | |
| 合　　計 | 7,595,379 | 4,960,000 | 執行期限： 107/06/01 ～ 108/05/31<br>計畫編號： MOST 107-2218-E-005-019 - |

研究類型：一般研究計畫(整合型)　　　　多年期計畫 學門名稱：人工智慧(AI on chip) 流水號： 107PFA0550661
研究性質：技術發展　　　　　　　　　　　　　　　　　　　　　　　　　　　　承辦人： 黃士育
應繳報告：期中進度報告(請於計畫執行期滿前二個月，至本部網站線上繳交進度報告，以憑核定下年度經費)
研究成果歸屬：國立中興大學
各項費用之支用請依「科技部補助專題研究計畫經費處理原則」規定辦理。

張振豪

# 中華民國專利證書

發明第　Ｉ781459　號

發 明 名 稱：手掌靜脈特徵辨識系統及其方法

專 利 權 人：國立中興大學

發 明 人：張振豪、陳泓烈

專利權期間：　自2022年10月21日至2040年10月 7 日止

上開發明業經專利權人依專利法之規定取得專利權

經濟部智慧財產局 局長　　洪淑敏

此證書為影本
正本留存學校

張振豪

中華民國　111　年　10　月　21　日

# 中華民國專利證書

發明第　　Ｉ758665　　號

發 明 名 稱：狀態辨識系統與方法

專 利 權 人：國立中興大學

發 明 人：張振豪、李欣翰、馬德芸

專利權期間：自2022年 3 月21日至2039年12月 4 日止

上開發明業經專利權人依專利法之規定取得專利權

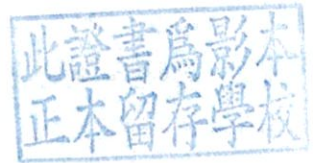經濟部智慧財產局 局長　　洪淑敏

中華民國 111 年 3 月 21 日

# 中華民國專利證書

## 發明第　I739634　號

發 明 名 稱：電力變壓器之故障診斷監控系統

專 利 權 人：國立中興大學

發 明 人：張振豪、王佳裕

專利權期間：　自 2021 年 9 月 11 日至 2040 年 10 月 15 日止

上開發明業經專利權人依專利法之規定取得專利權

經濟部智慧財產局 局長　　　　　洪淑敏　　　　　　張振豪

中華民國 110 年 9 月 11 日

注意：專利權人未依法繳納年費者，其專利權自原繳費期限屆滿後消滅。

# 中華民國專利證書

發明第　Ｉ731511　號

發 明 名 稱：指／掌靜脈辨識處理及其神經網路訓練方法

專 利 權 人：國立中興大學

發 明 人：張振豪、張智瑋、王佳裕

專利權期間： 自 2021 年 6 月 21 日至 2039 年 12 月 11 日止

上開發明業經專利權人依專利法之規定取得專利權

此證書為影本
正本留存學校

經濟部智慧財產局 局長　　洪淑敏
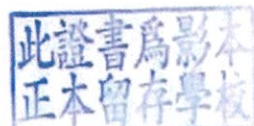
張振豪

中華民國 110 年 6 月 21 日

# 中華民國專利證書

## 發明第 I677179 號

發　明　名　稱：全整合主動式交流轉直流整流器

專　利　權　人：國立中興大學

發　明　　　人：張振豪、陳威志、劉霖

專利權期間：自 2019 年 11 月 11 日至 2038 年 11 月 28 日止

上開發明業經專利權人依專利法之規定取得專利權

經濟部智慧財產局 局長　　洪淑敏

此證書為影本
正本留存學校

張振豪

中華民國　108　年　11　月　11　日

注意：專利權人未依法繳納年費者，其專利權自原繳費期限屆滿後消滅。

# 個人資料提供同意書

　　本同意書說明國立中興大學（以下簡稱本校）將如何處理本表單所蒐集到的個人資料。當您勾選「我同意」並簽署本同意書時，表示您已閱讀、瞭解並同意接受本同意書之所有內容及其後修改變更規定。若您未滿二十歲，應於您的法定代理人閱讀、瞭解並同意本同意書之所有內容及其後修改變更規定後，方得使用本服務，但若您已接受本服務，視為您已取得法定代理人之同意，並遵守以下所有規範。

## 一、 基本資料之蒐集、更新及保管

1. 本校蒐集您的個人資料在中華民國「個人資料保護法」與相關法令之規範下，依據國立中興大學(以下簡稱本校)【隱私權政策聲明】，蒐集、處理及利用您的個人資料。

2. 請於申請時提供您本人正確、最新及完整的個人資料。

3. 本校因執行電機資訊學院院長遴選業務所蒐集您的個人資料包括姓名、性別、身分證或護照號碼、出生年月日、國 籍、職稱、聯絡方式(通訊處、電話、傳真、E-Mail)、學經歷等。

4. 若您的個人資料有任何異動，請主動向本校申請更正，使其保持正確、最新及完整。

5. 若您提供錯誤、不實、過時或不完整或具誤導性的資料，您將損失相關權益。

6. 您可依中華民國「個人資料保護法」，就您的個人資料行使以下權利：

(1) 請求查詢或閱覽。 (2) 製給複製本。(3) 請求補充或更正。 (4) 請求停止蒐集、處理及利用。

(5) 請求刪除。

但因本校執行職務或業務所必須者，本校得拒絕之。若您欲執行上述權利時，請參考本校【隱私權政策聲明】之個人資料保護聯絡窗口聯繫。但因您行使上述權利，而導致權益受損時，本校將不負相關賠償責任。

## 二、蒐集個人資料之目的

1. 本校為執行電機資訊學院院長遴選業務需蒐集您的個人資料。

2. 當您的個人資料使用方式與當初本校蒐集的目的不同時，我們會在使用前先徵求您的書面同意，您可以拒絕向本校提供個人資料，但您可能因此喪失您的權益。

3. 本校利用您的個人資料期間為入學日起至畢業。

## 三、基本資料之保密

您的個人資料受到本校【隱私權政策聲明】之保護及規範。本校如違反「個人資料保護法」規定或因天災、事變或其他不可抗力所致者，致您的個人資料被竊取、洩漏、竄改、遭其他侵害者，本校將於查明後以電話、信函、電子郵件或網站公告等方法，擇適當方式通知您。

## 四、同意書之效力

1. 當您勾選「我同意」並簽署本同意書時，即表示您已閱讀、瞭解並同意本同意書之所有內容，您如違反下列條款時，本校得隨時終止對您所提供之所有權益或服務。

2. 本校保留隨時修改本同意書規範之權利，本校將於修改規範時，公告修改之事實，不另作個別通知。如果您不同意修改的內容，請勿繼續接受本服務。否則將視為您已同意並接受本同意書該等增訂或修改內容之拘束。

3. 您自本同意書取得的任何建議或資訊，無論是書面或口頭形式，除非本同意書條款有明確規定，均不構成本同意條款以外之任何保證。

## 五、準據法與管轄法院

本同意書之解釋與適用，以及本同意書有關之爭議，均應依照中華民國法律予以處理，並以臺灣臺中地方法院為管轄法院。

■我已閱讀並接受上述同意書內容

當事人簽名(請親簽)： 張振豪

法定代理人簽名(請親簽)：

113 年 4 月 15 日

# 教授證書

教字第 〇一二八三〇 號

姓名：張振豪

身分證字號：

出生年月日：伍拾肆年伍月貳■日

年資起算：玖拾貳年捌月

送審學校：國立中興大學

經本部依專科以上學校教師資格審定辦法審定合於教授資格此證

教育部部長 黃榮村

中華民國玖拾貳年捌月壹拾捌日

張振豪

# University of Southern California

The Trustees of the University by virtue of the authority vested
in them and on the recommendation of the faculty of

## The Graduate School

have conferred the degree of

## Doctor of Philosophy

### Electrical Engineering

on

## Robert Chen-Hao Chang

Given at Los Angeles, California, on the twelfth day of May, in the year
one thousand nine hundred and ninety-five

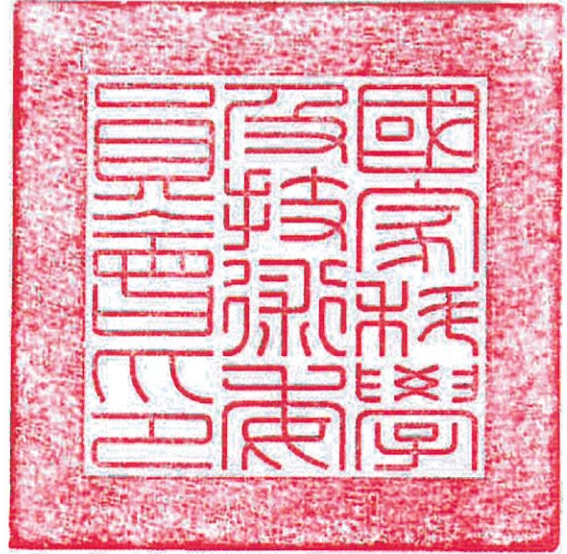President of the University

Chairman of the Board of Trustees

Dean

張振豪

檔　號：

保存年限：

# 國家科學及技術委員會　聘函

地址：臺北市大安區和平東路二段106號
電話：02-2737-7208

402202　P2-掛號
國立中興大學電機工程學系（所）
臺中市南區興大路145號
受文者：張振豪教授

發文日期：中華民國113年1月23日

發文字號：科會人字第1130005901號

速別：普通件

密等及解密條件或保密期限：

附件：

　　茲　聘

臺端為本會工程技術研究發展處微電子學門召集人，聘期自113
年1月1日起至113年12月31日止。

正本：張振豪教授
副本：本會工程處、人事處

主任委員　吳政忠

# 國家科學及技術委員會　聘函

40227　P3-限時掛號
國立中興大學電機工程學系（所）
臺中市南區興大路145號
受文者：國立中興大學電機工程學系
　　　　（所）張振豪教授

發文日期：中華民國112年5月10日

發文字號：科會前字第1120027387B號

速別：普通件

密等及解密條件或保密期限：

附件：

　茲　聘

臺端為本會國家核心關鍵技術諮詢委員，聘期自112年5月10日至
114年5月9日止。

正本：國立中興大學電機工程學系（所）張振豪教授
副本：本會前瞻應用處

主任委員　吳政忠

張振豪

檔　　號：
保存年限：

# 國家科學及技術委員會　聘函

地址：臺北市和平東路二段106號
電話：02-2737-7538

40227　P3-限時掛號
國立中興大學電機工程學系（所）
臺中市南區興大路145號
受文者：張振豪委員
發文日期：中華民國111年10月3日
發文字號：科會前字第1110061405號
速別：普通件
密等及解密條件或保密期限：
附件：

　　茲　聘

臺端為本會「臺灣AI卓越中心(Taiwan AICoE)策略委員會」委員，聘期自111年10月1日至113年9月30日止。

正本：張振豪委員
副本：本會前瞻應用處

主任委員　吳政忠

張振豪

檔　號：
保存年限：

# 國家科學及技術委員會　函

地址：臺北市和平東路二段106號
聯絡人：孔德靜　研究員
電話：02-2737-7024
傳真：
電子信箱：tckung@nstc.gov.tw

402202　P3-限時掛號
國立中興大學電機工程學系（所）
臺中市南區興大路145號
受文者：國立中興大學電機工程學系
　　　　（所）教授張振豪

發文日期：中華民國113年1月24日
發文字號：科會科辦字第1130006207A號
速別：普通件
密等及解密條件或保密期限：
附件：

主旨：茲敦聘台端兼任本會「科技政策諮詢專家室」之領域群組
　　　領域專家，任期自113年1月1日至113年12月31日止。

說明：

一、為精進我國科研計畫管理評估及提供國家中長程科技政策
　　觀察建言，延攬優秀科技管理人才以全程重點式深入參與
　　重大科技計畫之審議與管理，及精進國家科技政策治理與
　　國家創新競爭力，本會科技辦公室推動成立「科技政策諮
　　詢專家室」。

二、台端聘任期間倘另兼任中高階行政主管職務，為兼顧專家
　　本職與本計畫兼職之任務，並考量本計畫職務性質尚具利
　　益迴避之必要，將視情形予以終止聘任本計畫之兼職。

正本：國立中興大學電機工程學系（所）教授張振豪
副本：國立中興大學、本會科技辦公室

主任委員　吳政忠

張振豪

# 國家科學及技術委員會　函

機關地址：台北市和平東路二段106號
聯絡人：鄭欣庭
電話：(02)27377727
傳真：(02)27377733
電子信箱：htcheng3@nstc.gov.tw

受文者：國立中興大學電機工程學系教授張振豪

發文日期：中華民國112年1月7日
發文字號：科會科辦字第1120002061E號
速別：普通件
密等及解密條件或保密期限：
附件：

主旨：茲敦聘台端兼任本會科技辦公室推動「邁向智慧國家決
　　　策支援暨科技計畫推動諮詢計畫」下成立「科技政策諮
　　　詢專家室」之領域群組領域專家，任期自112年1月7日至
　　　112年12月31日止。

說明：

一、旨揭計畫係為精進我國科研計畫管理評估及提供國家中
　　長程科技政策觀察建言，延攬優秀科技管理人才以全程
　　重點式深入參與重大科技計畫之審議與管理，及精進國
　　家科技政策治理與國家創新競爭力。

二、台端聘任期間倘另兼任中高階行政主管職務，為兼顧專
　　家本職與本計畫兼職之任務，並考量本計畫職務性質尚
　　具利益迴避之必要，將視情形予以終止聘任本計畫之兼
　　職。

正本：國立成功大學牙醫學系講座教授謝達斌、臺北醫學大學大數據科技及管理研究
　　　所所長許明暉、國立成功大學生物化學暨分子生物學研究所所長莊偉哲、國立
　　　臺灣大學農藝學系教授王淑珍、國立臺灣大學動物科學技術學系教授劉嘉睿、
　　　國立臺灣大學材料科學與工程學系特聘教授高振宏、國立臺灣大學化學工程學
　　　系教授吳嘉文、國立臺北科技大學土木工程系特聘教授林鎮洋、國立中興大學
　　　電機工程學系教授張振豪、財團法人台灣網路資訊中心董事暨執行長黃勝雄、
　　　國立成功大學資訊工程學系副教授莊坤達、國立臺灣大學資訊工程學系教授楊
　　　佳玲、國立臺灣大學電機工程學系教授魏宏宇、國立臺灣大學機械工程學系終
　　　身特聘教授陳炳輝、國立政治大學財政學系教授連賢明、國立清華大學跨院國
　　　際博士班學位學程合聘教授陳珠櫻、國立成功大學創意產業設計研究所副教授

國立中興大學

第1頁，共2頁

1120000490　112-01-07

電資學院

# 國家科學及技術委員會　函

受文者：國立中興大學電機工程學系張振豪教授

發文日期：中華民國111年8月3日
發文字號：科會科辦字第1110049966號
速別：普通件
密等及解密條件或保密期限：
附件：

主旨：茲敦聘台端兼任本辦公室推動「科技決策支援暨科技計
　　　畫推動諮詢計畫」下成立「科技政策諮詢專家室」之領
　　　域專家群一員，任期自111年8月1日至111年12月31日
　　　止。

說明：

一、旨揭計畫係為精進我國科研計畫管理評估及提供國家中
　　長程科技政策觀察建言，延攬優秀科技管理人才以全程
　　重點式深入參與重大科技計畫之審議與管理，及精進國
　　家科技政策治理與國家創新競爭力。

二、台端聘任期間倘另兼任中高階行政主管職務，為兼顧專
　　家本職與本計畫兼職之任務，並考量本計畫職務性質尚
　　具利益迴避之必要，將視情形予以終止聘任本計畫之兼
　　職。

正本：財團法人中華經濟研究院第二研究所陳信宏所長、國立中興大學電機工程學系
　　　張振豪教授
副本：國立中興大學、本會科技辦公室

主任委員吳政忠

張振豪

第1頁，共1頁

1110014921　111-08-03

# 國立暨南國際大學服務證明書

| 姓　　　　名 | 張振豪 | 身分證統一編號 | ■■■■■■ | |
|---|---|---|---|---|
| 性　　　　別 | 男 | 出生年月日 | 民國 54 年 05 月 ■ 日 | |
| 歷　　　年　　　所　　　任　　　工　　　作 | | | | |
| 職　　　　稱 | 教授 | | | |
| 職　務　列　等 | 本薪 475-680 年功最高薪 770 | | | |
| 任　職　日　期 | 103 年 08 月 01 日 | | | |
| 卸　職　日　期 | 106 年 08 月 01 日 | | | |
| 卸　職　原　因 | 借調期滿歸建 中興大學 | | | |
| 體階或薪額 | 770 薪點 | | | |
| 備　　　　註 | 1. 張師自 103 年 8 月 1 日至 106 年 7 月 31 日止兼任本校前瞻性高科技研究中心中心主任職務。 2. 張師自 103 年 8 月 1 日至 106 年 7 月 31 日止兼任本校科技學院院長職務。 3. 張師於本校任教期間服務成績優良。 | | | |

上表所列各項均經查明屬實，特予證明。

上給

張振豪　君收執

校長蘇玉龍

張振豪

中　華　民　國　1　0　6　年　0　8　月　0　1　日

# NARLabs

## 財團法人國家實驗研究院
### National Applied Research Laboratories

感謝 張振豪副主任
費心協助晶片中心業務

# 功績卓著

國家晶片系統設計中心
主任 闕志達 敬贈
103 年 1 月

張振豪

**◆IEEE**

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*IEEE hereby expresses its appreciation for*
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*towards the advancement of*
*IEEE and the Engineering Professions to*

Chen-Hao Chang

Chair

Circuits and Systems Society Chapter
Taipei Section
2011-2012

Fred Mintzer
Vice President, Technical Activities

Howard E. Michel
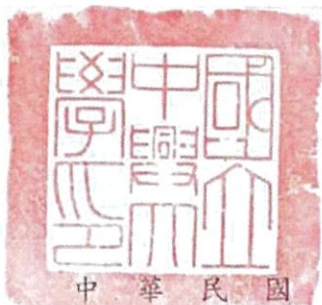Vice President, Member and Geographic Activities

張振豪

國立中興大學聘函 （95）校人聘行字第 100 號

敬　聘

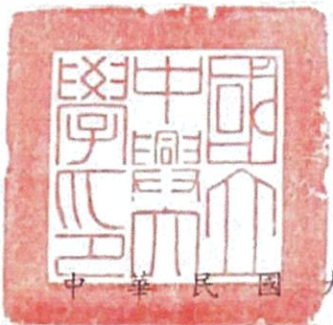張振豪教　授兼任本校工學院電機工程學系系
主任，聘期自九十五年八月一日起至九十六年
七月三十一日止。

此聘

校　長　蕭介夫

中　華　民　國　九十五　年　七　月　　日

---

國立中興大學聘函 （96）校人聘行字第 063 號

敬　聘

張振豪教　授兼任本校工學院電機工程學系系
主任，聘期自九十六年八月一日起至九十七年
七月三十一日止。

此聘

校　長　蕭介夫

中　華　民　國　九十六　年　七　月　　日
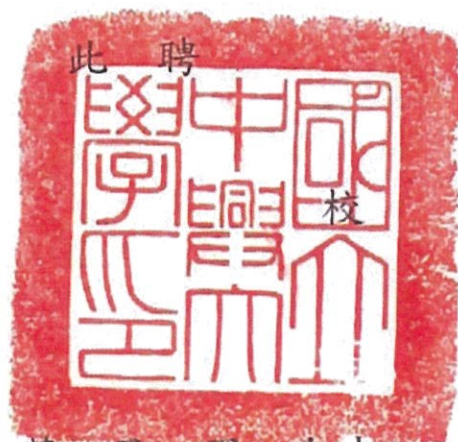
張振豪

國立中興大學聘函　　（94）工科發第 001 號

敬　聘

張振豪教　授兼任本校工學院工程科技研發中心主任，聘期自九十四年八月一日起至九十五年七月三十一日止。

此聘

校　長　蕭介夫

中　華　民　國　九十四　年　九　月　日

張振豪

國立中興大學聘書　（一）85校人聘兼字第386號

敬聘

張振豪先生為本大學工學院電機工程學系

副教授，聘期自捌拾伍年捌月壹日起至

捌拾陸年柒月底止。

校長　黃東熊
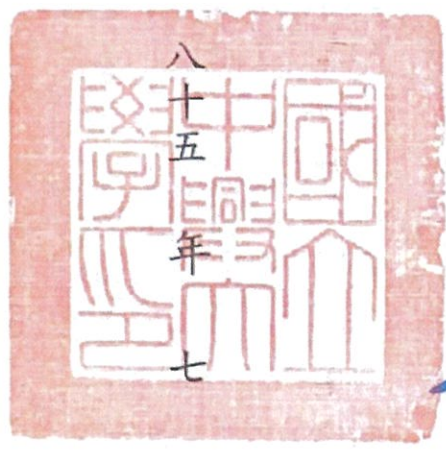
中華民國八十五年七月　　日

張振豪

傑出電機工程教授獎

本會會員 張振豪 博士

對我國電機工程教育

有傑出貢獻，經本會

評定，特頒獎狀，以

資鼓勵。

中華民國一〇九年十二月十八日

中國電機工程學會

理事長 周景揚

**The Chinese Institute of Electrical Engineering**

**Outstanding Electrical Engineering Professor Award**

This citation is presented to the member of CIEE

Dr. Robert Chen-Hao Chang

to recognize his excellent contributions

to education of electrical engineering

*Jing-Yang Jou*

President

Dec. 18, 2020

國立中興大學

# 國立中興大學　聘書

終特字第 75 號

茲敦聘

張振豪 教授為本校終身特聘教授

此聘

校　長　薛富盛

張振豪

中華民國一百零九年九月　日

# 感 謝

## 中興大學張振豪教授

研究團隊執行「智慧行車安全監控
嵌入式系統設計」

## 績效卓著

計畫總主持人 陳文村

中華民國 104 年 12 月 22 日

張振豪

**IEEE CASS DLP 網頁公告：**
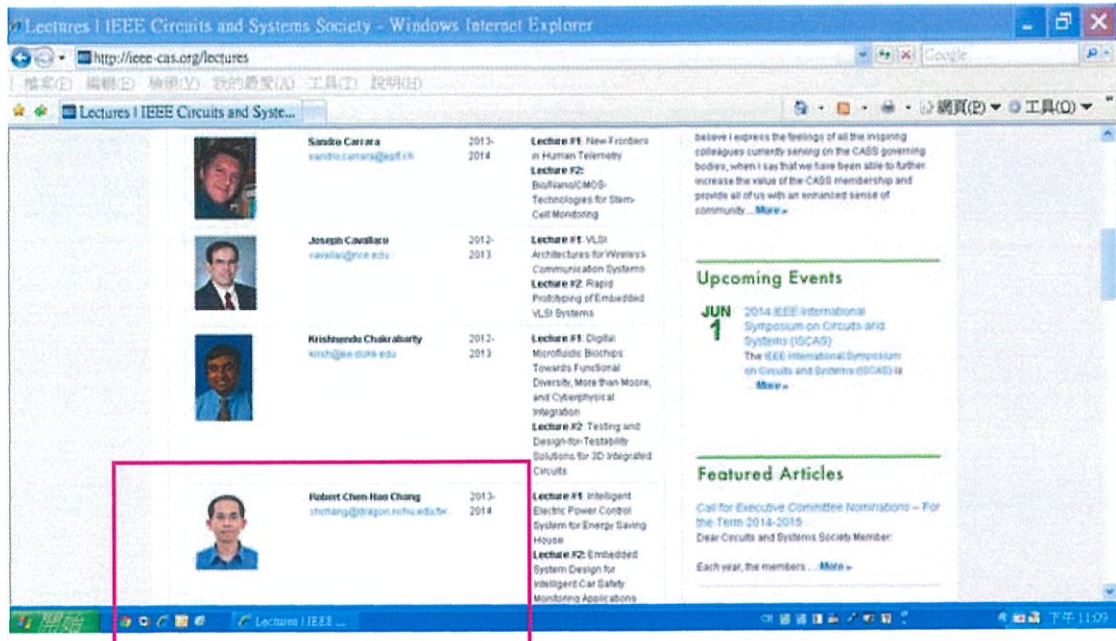
# 聘　書

特聘字第 165 號　　　　　　　　　　　　2012 年 2 月 1 日

茲敦聘

張振豪 教授爲本校

特聘教授

聘期自 2012 年 2 月 1 日至 2014 年 1 月 31 日

謹此至表尊崇

國立中興大學校長　李德財

張振豪

國立中興大學
NATIONAL CHUNG HSING UNIVERSITY

# 聘　　書
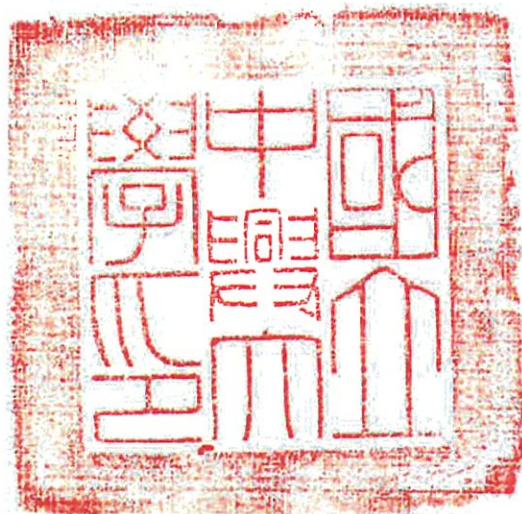
2014 年 2 月 1 日

茲 敦 聘

張 振 豪　教 授 為 本 校

特 聘 教 授

聘期自 2014 年 2 月 1 日至 2016 年 1 月 31 日

謹 此 至 表 尊 崇

國立中興大學校長　李德財

張振豪

國立中興大學

# 聘　書

特聘字第 543 號

茲　敦　聘

張　振　豪　教　授　為　本　校

特　聘　教　授

聘期自 109 年 8 月 1 日至 111 年 7 月 31 日

謹　此　至　表　尊　崇

國立中興大學校長　薛富盛

中　華　民　國　109　年　9　月　日

國立中興大學
1919

# 聘　　書

特聘字第 626 號

茲 敦 聘

張 振 豪 教 授 為 本 校

特 聘 教 授

聘期自 111 年 8 月 1 日至 113 年 7 月 31 日

謹 此 至 表 尊 崇

國立中興大學校長　薛富盛

中 華 民 國 111 年 9 月　日

# Fellow of IET 獲選通知：

# IET Fellow

## Forward Thinking

Ref: FIET10F/1100219612
26 September 2011

Professor R Chang FIET

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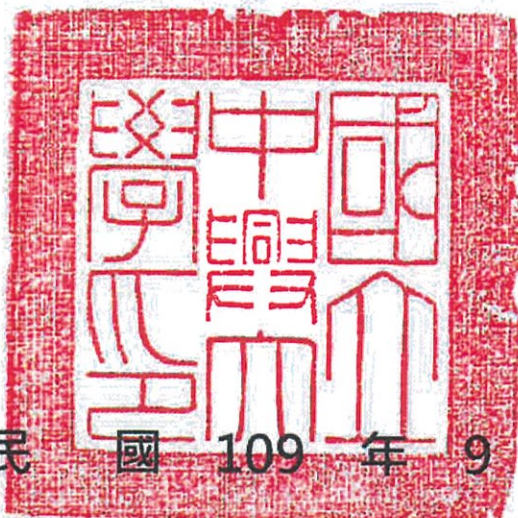Taichung
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Taiwan, Republic of China

Institution of Engineering a Technology

Michael Faraday House

Six Hills Way

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Hertfordshire SG1 2AY

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F +44 (0)1438 765526

E fellowship@theiet.org

www.theiet.org

Dear Professor Chang

I am delighted to inform you that your application for admission to Fellowship of the Institution of Engineering and Technology (the IET) has been approved, with effect from the date of this letter.

I hope that your Fellowship will be a source of satisfaction to you as well as a benefit to the profession and the community we serve. Fellowship is recognition of your professional achievement and I hope that you will be able to share this experience through your participation and contribution to the IET's activities. The IET has a global membership and your support for your local region will be most welcome.

I would particularly encourage you to identify, motivate and support your colleagues and associates who you believe would be suitable candidates for Fellowship.

The IET promotes newly elected Fellows on the website www.theiet.org/newfellow, the month following election and also in the next edition of Members' News. A twice yearly listing also appears in The Times and you will be notified of this nearer its publication. If you do not wish to be included please contact pdinner@theiet.org for removal from these listings.

A new card, showing your Fellowship to the IET, will be automatically ordered and sent to you. Fellow ties can be purchased for £25.00 by contacting Member & Customer Service on telephone number +44 (0)1438 765678.

I welcome you as a Fellow and look forward to working with you to promote the IET as the professional home for life for engineers and technicians.

Yours sincerely

Nigel Fine BSc MBA CEng FICE FIET
Chief Executive and Secretary

張振豪

行政院國家科學委員會100年度補助大專校院獎勵特殊優秀人才措施獎勵名冊

機構名稱：國立中興大學
計畫編號：100-3114-C-005-001-ES

單位：新台幣元

| 序號 | 姓名 | 職稱 | 系所名稱 | 現職/新聘 | 每月獎勵金額(A) | 獎勵月數(B) | 小計(A*B) | 補助經費總額 | 第1期款(100年8月至101年1月) | 第2期款(101年2月至101年7月) | 歸屬處別 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 廖思善 | 特聘教授II | 物理系 | 現職 | 25,000 | 12 | 300,000 | 300,000 | 150,000 | 150,000 | 自然處 |
| 2 | 林勳億 | 特聘教授II | 化學系 | 現職 | 25,000 | 12 | 300,000 | 300,000 | 150,000 | 150,000 | 自然處 |
| 3 | 林寬鋸 | 特聘教授II | 化學系 | 現職 | 25,000 | 12 | 300,000 | 300,000 | 150,000 | 150,000 | 自然處 |
| 4 | 葉鎮宇 | 特聘教授II | 化學系 | 現職 | 25,000 | 12 | 300,000 | 300,000 | 150,000 | 150,000 | 自然處 |
| 5 | 洪豐裕 | 特聘教授II | 化學系 | 現職 | 25,000 | 12 | 300,000 | 300,000 | 150,000 | 150,000 | 自然處 |
| 6 | 周三和 | 特聘教授 | 生化所 | 現職 | 50,000 | 12 | 600,000 | 600,000 | 300,000 | 300,000 | 自然處 |
| 7 | 俞慧芝 | 特聘教授 | 生科系 | 現職 | 25,000 | 12 | 300,000 | 300,000 | 150,000 | 150,000 | 自然處 |
| 8 | 莊榮厚 | 產學績優教授II | 環工系 | 現職 | 20,000 | 12 | 240,000 | 240,000 | 120,000 | 120,000 | 自然處 |
| 9 | 楊國賜 | 產學績優教授II | 化學系 | 現職 | 10,000 | 12 | 120,000 | 120,000 | 60,000 | 60,000 | 自然處 |
| 10 | 楊吉斯 | 產學績優教授II | 昆蟲系 | 現職 | 10,000 | 12 | 120,000 | 120,000 | 60,000 | 60,000 | 自然處 |
| 11 | 彭宗仁 | 產學績優教授II | 土環系 | 現職 | 10,000 | 12 | 120,000 | 120,000 | 60,000 | 60,000 | 自然處 |
| 12 | 林俊良 | 講座教授 | 電機系 | 現職 | 60,000 | 12 | 720,000 | 420,000 | 210,000 | 210,000 | 工程處 |
| 13 | 黃博惠 | 特聘教授II | 資工系 | 現職 | 40,000 | 12 | 480,000 | 480,000 | 240,000 | 240,000 | 工程處 |
| 14 | 魏銘志 | 特聘教授II | 環工系 | 現職 | 40,000 | 12 | 480,000 | 480,000 | 240,000 | 240,000 | 工程處 |
| 15 | 楊谷章 | 特聘教授II | 電機系 | 現職 | 40,000 | 12 | 480,000 | 480,000 | 240,000 | 240,000 | 工程處 |
| 16 | 蔡清池 | 特聘教授II | 電機系 | 現職 | 40,000 | 12 | 480,000 | 480,000 | 240,000 | 240,000 | 工程處 |
| 17 | 洪振義 | 特聘教授 | 醫工所 | 現職 | 40,000 | 12 | 480,000 | 480,000 | 240,000 | 240,000 | 工程處 |
| 18 | 李學斛 | 特聘教授II | 環工系 | 現職 | 25,000 | 12 | 300,000 | 300,000 | 150,000 | 150,000 | 工程處 |
| 19 | 林其璋 | 特聘教授II | 土木系 | 現職 | 25,000 | 12 | 300,000 | 300,000 | 150,000 | 150,000 | 工程處 |
| 20 | 薛富盛 | 特聘教授II | 材料系 | 現職 | 25,000 | 12 | 300,000 | 300,000 | 150,000 | 150,000 | 工程處 |
| 21 | 鄧俊明 | 特聘教授II | 化工系 | 現職 | 25,000 | 12 | 300,000 | 300,000 | 150,000 | 150,000 | 工程處 |
| 22 | 王國禎 | 特聘教授II | 機械系 | 現職 | 25,000 | 12 | 300,000 | 300,000 | 150,000 | 150,000 | 工程處 |
| 23 | 莊家峰 | 特聘教授II | 電機系 | 現職 | 25,000 | 12 | 300,000 | 300,000 | 150,000 | 150,000 | 工程處 |
| 24 | 呂福興 | 特聘教授II | 材料系 | 現職 | 25,000 | 12 | 300,000 | 300,000 | 150,000 | 150,000 | 工程處 |
| 25 | 楊錫杭 | 特聘教授II | 精密所 | 現職 | 25,000 | 12 | 300,000 | 300,000 | 150,000 | 150,000 | 工程處 |
| 26 | 林慶炫 | 特聘教授II | 化工系 | 現職 | 25,000 | 12 | 300,000 | 300,000 | 150,000 | 150,000 | 工程處 |
| 27 | 吳威德 | 產學績優教授II | 材料系 | 現職 | 20,000 | 12 | 240,000 | 240,000 | 120,000 | 120,000 | 工程處 |
| 28 | 陳獻吉 | 產學績優教授II | 土木系 | 現職 | 20,000 | 12 | 240,000 | 240,000 | 120,000 | 120,000 | 工程處 |
| 29 | 張振豪 | 產學績優教授II | 電機系 | 現職 | 20,000 | 12 | 240,000 | 240,000 | 120,000 | 120,000 | 工程處 |
| 30 | 盧昭榮 | 產學績優教授II | 土木系 | 現職 | 20,000 | 12 | 240,000 | 240,000 | 120,000 | 120,000 | 工程處 |
| 31 | 盧重興 | 產學績優教授II | 環工系 | 現職 | 10,000 | 12 | 120,000 | 120,000 | 60,000 | 60,000 | 工程處 |
| 32 | 吳宗明 | 產學績優教授II | 材料系 | 現職 | 10,000 | 12 | 120,000 | 120,000 | 60,000 | 60,000 | 工程處 |
| 33 | 黃介辰 | 產學績優教授II | 生科系 | 現職 | 10,000 | 12 | 120,000 | 120,000 | 60,000 | 60,000 | 工程處 |
| 34 | 蔡清標 | 產學績優教授II | 土木系 | 現職 | 10,000 | 12 | 120,000 | 120,000 | 60,000 | 60,000 | 工程處 |
| 35 | 盧秋坊 | 產學績優教授II | 機械系 | 現職 | 10,000 | 12 | 120,000 | 120,000 | 60,000 | 60,000 | 工程處 |
| 36 | 楊明德 | 產學績優教授II | 土木系 | 現職 | 10,000 | 12 | 120,000 | 120,000 | 60,000 | 60,000 | 工程處 |
| 37 | 楊秋忠 | 中興講座 | 土環系 | 現職 | 90,000 | 12 | 1,080,000 | 580,000 | 290,000 | 290,000 | 生物處 |
| 38 | 葉鍚東 | 中興講座 | 植病系 | 現職 | 80,000 | 12 | 960,000 | 960,000 | 480,000 | 480,000 | 生物處 |
| 39 | 顏國欽 | 講座教授 | 食科系 | 現職 | 60,000 | 12 | 720,000 | 720,000 | 360,000 | 360,000 | 生物處 |
| 40 | 李佩珊 | 講座教授 | 獸醫系 | 現職 | 60,000 | 12 | 720,000 | 720,000 | 360,000 | 360,000 | 生物處 |
| 41 | 毛正倫 | 特聘教授 | 食生系 | 現職 | 50,000 | 12 | 600,000 | 300,000 | 150,000 | 150,000 | 生物處 |
| 42 | 曾志正 | 特聘教授 | 生技所 | 現職 | 50,000 | 12 | 600,000 | 600,000 | 300,000 | 300,000 | 生物處 |
| 43 | 楊長賢 | 特聘教授II | 生科所 | 現職 | 40,000 | 12 | 480,000 | 480,000 | 240,000 | 240,000 | 生物處 |
| 44 | 孟孟孝 | 特聘教授II | 生技所 | 現職 | 40,000 | 12 | 480,000 | 480,000 | 240,000 | 240,000 | 生物處 |
| 45 | 黃振文 | 特聘教授 | 植病系 | 現職 | 25,000 | 12 | 300,000 | 300,000 | 150,000 | 150,000 | 生物處 |
| 46 | 陳櫻群 | 特聘教授 | 水保系 | 現職 | 25,000 | 12 | 300,000 | 300,000 | 150,000 | 150,000 | 生物處 |
| 47 | 鄧裕民 | 特聘教授 | 土環系 | 現職 | 25,000 | 12 | 300,000 | 300,000 | 150,000 | 150,000 | 生物處 |
| 48 | 王升陽 | 特聘教授 | 森林系 | 現職 | 25,000 | 12 | 300,000 | 300,000 | 150,000 | 150,000 | 生物處 |
| 49 | 周志輝 | 特聘教授 | 食生系 | 現職 | 25,000 | 12 | 300,000 | 300,000 | 150,000 | 150,000 | 生物處 |
| 50 | 謝慶昌 | 特聘教授 | 生技所 | 現職 | 25,000 | 12 | 300,000 | 300,000 | 150,000 | 150,000 | 生物處 |
| 51 | 胡淼琳 | 特聘教授 | 食生系 | 現職 | 25,000 | 12 | 300,000 | 300,000 | 150,000 | 150,000 | 生物處 |
| 52 | 黃晶柱 | 特聘教授 | 動科系 | 現職 | 25,000 | 12 | 300,000 | 300,000 | 150,000 | 150,000 | 生物處 |
| 53 | 王蓮祥 | 特聘教授 | 生技所 | 現職 | 25,000 | 12 | 300,000 | 300,000 | 150,000 | 150,000 | 生物處 |
| 54 | 方繼 | 特聘教授 | 食生系 | 現職 | 25,000 | 12 | 300,000 | 300,000 | 150,000 | 150,000 | 生物處 |
| 55 | 陳鑾釧 | 特聘教授 | 生醫所 | 現職 | 50,000 | 12 | 600,000 | 300,000 | 150,000 | 150,000 | 生物處 |

張振豪

# 獎　狀

（九十八）興電字第一○○一號

張振豪 教授榮獲九十八學年度

國立中興大學電機工程學系

優良教師評選　第一名　特頒

此狀以資表揚

校長　<signature>
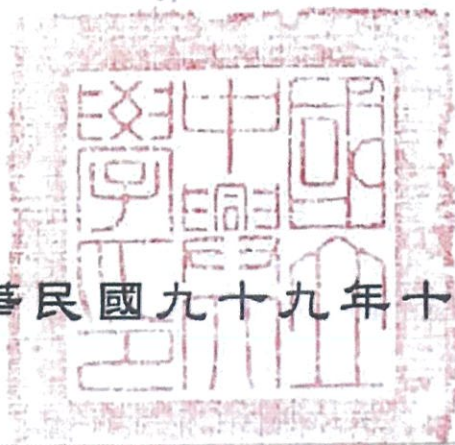
中華民國九十九年十一月

# 國立中興大學工學院　書函

受文者：電機工程學系

主　　旨：台端榮獲 98 學年度「工學院產學合作優良獎」，請　查照。

說　　明：依據本院 98 年 9 月 15 日召開「工學院 98 學年度第二次學術委員會」
　　　　　決議辦理。

正本：土木系蔡清標教授、蘇苗彬教授；機械系戴慶良教授、機械系蔡志成副教
　　　授；環工系李季眉教授、盧重興教授、莊秉潔教授；電機系張振豪教授、
　　　林俊良教授；材料系顏秀崗教授、吳宗明教授、汪俊延副教授、林佳鋒副
　　　教授；精密所韓斌教授

副本：土木系、機械系、環工系、電機系、材料系、精密所

# 工　學　院

張振豪

## 國立中興大學工學院　書函

聯絡人：陳莉莉（430 轉 308）

受文者：電機工程學系－張振豪教授

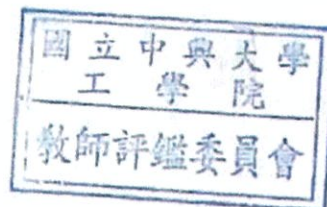發文日期：中華民國 98 年 5 月 27 日
發文字號：興工瑋字第 98-035 號
速別：
密等及解密條件或保密期限：密件
附件：

主旨：台端經本院九十七學年度教師評鑑結果，獲評為「評鑑特優」教師，
　　　請 查照。

說明：依據本院九十八年五月二十二日召開「九十七學年度工學院第二次
　　　教師評鑑委員會議」決議辦理。

正本：張振豪老師、顏秀崗老師

副本：電機系、材料系

# 工學院教師評鑑委員會

國立中興大學
工 學 院
教師評鑑委員會

張振豪

國立中興大學

敬賀 張教授 振豪 榮獲
九十四年度建教合作研究計畫

績優獎

校長 蕭介夫 敬贈
中華民國九十五年九月

張振豪

國立中興大學

九十二學年度
教學特優教師獎

電機工程學系　　張振豪　教授

於 本 校 服 務 期 間 教 學 表 現
卓 著 足 堪 表 率 特 頒 獎 狀 誌 念

此 狀

國立中興大學校長

中 華 民 國 九 十 三 年 五 月 六 日

# Distinguished Teaching Award

This Award is Presented to

Prof./Dr./Mr./Ms. __CHEN-HAO CHANG__

A Faculty Member of

__DEPARTMENT OF ELECTRICAL ENGINEERING__

In Recognition of his /her Great Dedication and

Outstanding Achievement in Pedagogic Work

_____

President
National Chung-Hsing University
Date : __May    6    2004__

張振豪